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Graphdiyne for multilevel flexible organic resistive random access memory devices

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Graphdiyne (GD), a new carbon allotrope with a 2D structure comprising benzene rings and carbon–carbon triple bonds, is employed in fabricating resistive random access memory (RRAM) devices. On inserting a GD nanoparticle (NP) discontinuous layer and thermally depositing an Al–Al_2O_3 core–shell (Al–Al_2O_3) NP discontinuous layer in insulating polyimide (PI) films on a PET substrate, the designed flexible three-state memory device is realized (PET/Ag/PI/GD/PI/Al–Al_2O_3/PI/Al). GD NPs and Al–Al_2O_3 NPs function as two types of strong electron traps with different energy levels, resulting in two ON states. The OFF state and the two ON states possess long retention times of more than 10^4 s. Our results here demonstrate that GD could have great potential applications in future information storage technologies.

Conventional Si memory devices are currently approaching their scaling limits, and researchers are now enthusiastically developing new memory technologies to improve storage density and realize high-density integration.[1–5] Multilevel memory devices can realize multi-state storage, and hence emerge as one of most attractive technologies.[6–10] Moreover, resistive random access memory (RRAM) exploits the electric-field responsive resistive-switching of materials as an information write/erase principle for nonvolatile data storage;[11–14] this technology is attracting more and more attention in the memory field, particularly organic-based ones due to their low cost, high flexibility, and 3-dimensional storage capability. Organic-based RRAM is expected to provide fast switching and high-density data storage for next-generation novel memory applications,[15–18] and researchers have been trying various pathways to realize multi-states in organic-based RRAM systems.

Multilevel organic RRAM devices are generally fabricated based on a very fundamental architecture, namely a bottom electrode (BE)/active material/top electrode (TE) structure. In the early years, semiconductors were used as the active materials, and different conductive states were realized by controlling the filament formations under different bias sweeps.[19,20] Later, novel materials were synthesized to realize multilevel storage capability by photoelectronic doping[21,22] or electric-field-controllable doping.[23,24] Then, composites consisting of organic materials and core–shell nanoparticles (NPs) were used; this structure showed that a negative differential resistance (NDR) and a different sweeping voltage will result in a multistate property in the NDR process by trapping/detrapping.[25,26] Recently, researchers also fabricated multilevel devices through different traps induced by different dopants in the bulk materials.[27,28] However, all the mentioned processes that are responsible for the multistate properties (including filament formation, doping and trapping) in bulk-composites films cannot be well-controlled by the applied bias, leading to unsatisfactory reproducibility and stability.[29,30]

Forming different strong traps with different energy levels could be a feasible way to realize stable multilevel memory states.[31] In this study, we utilized two different types of NPs to form two carrier traps in the designed organic RRAM shown in Fig. 1a. Specifically, discontinuous graphdiyne (GD) NP and Al–Al_2O_3 core–shell (Al–Al_2O_3) NP layers are inserted in the polyimide (PI) layer. From SEM images it is observed that both the GD layer (Fig. 1b) and Al–Al_2O_3 layer (Fig. 1c) are discontinuous and

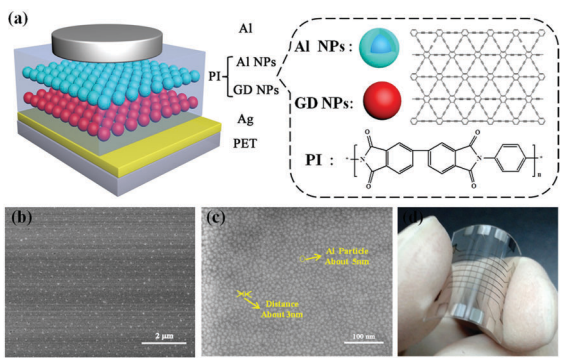

Fig. 1 (a) Schematic of the fabricated RRAM. The insets are the structure diagram and the molecular structure of the used materials. (b) SEM image of the spin-coating GD NPs. (c) SEM image of the evaporated Al–Al_2O_3 core–shell NPs. (d) Photograph of the fabricated flexible RRAM.

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the two layers are well separated by the PI layers. The Ag bottom electrode (BE) and the Al top electrode (TE) serve as the anode and cathode, respectively. In such a structure (BE/PI/GD/PI/Al–Al_2O_3/PI/TE), the GD NPs and the Al–Al_2O_3 NPs are designed to act as two types of traps to generate multilevel memory states.

As a new carbon allotrope with a 2D structure comprising benzene rings and carbon–carbon triple bonds,[32] GD shows an excellent performance in lithium-ion batteries,[33] photodetectors[34] and solar cells.[35] Herein, GD NPs are designed to serve as a type of charge storage trap like graphene.[36] The GD powder was synthesized according to a procedure reported in literature.[32] The GD NP solution was prepared by dispersing the GD powder in chlorobenzene at a concentration of 1 mg ml^{-1} and was then ultrasonicated at 50 °C for more than a week. For the Al–Al_2O_3 core–shell NPs, the Al core is surrounded by a thin oxide shell of 1.5–2.0 nm.[37] Fig. 1d is a photograph of the fabricated flexible device on a polyethylene terephthalate (PET) substrate. All the devices in the manuscript were prepared by layer-by-layer processing. The PI films and GD NP film are solution processed (the solution concentration of PI in methyl-2-pyrrolidinone (NMP) is 10 mg ml^{-1} and GD in chlorobenzene is 1 mg ml^{-1}) by spin-coating their solutions at 2000 rpm for 5 seconds and subsequently at 2000 rpm for 35 seconds. The prepared PI film was soft-baked on a hot plate at 120 °C for 10 min (to dry the solvent and cross-link the PI molecules). The Al–Al_2O_3 core–shell NP film was prepared by the thermal deposition of 4 nm-thick Al onto the beneath PI layer at a deposition rate of 0.05 nm s^{-1}. Then, the Al NPs were exposed to air to form the Al–Al_2O_3 core–shell structure. The Ag and Al electrodes were thermally deposited with the help of a shadow mask at a deposition rate of 0.1 nm s^{-1}, resulting in a 100 μm × 100 μm device area. The two electrodes are both 50 nm-thick.

Fig. 2 shows the properties of four fabricated devices: the device without any NPs (BE/PI/TE), with only GD NPs (BE/PI/GD/PI/TE), with only Al–Al_2O_3 NPs (BE/PI/Al–Al_2O_3/PI/TE), and with both types of NPs (BE/PI/GD/PI/Al–Al_2O_3/PI/TE). It is seen that for the device without NPs (Fig. 2a), the *I–V* curve turned out to be smooth for both biasing directions, indicating that the device has no memory function. For the device with GD NPs (Fig. 2b) and the device with Al–Al_2O_3 NPs (Fig. 2c), they both present a bistable memory property during the bias sweep. The setting voltage is around 1.5 V for the GD based device, and is around 3 V for the Al–Al_2O_3 based device. This larger set voltage for the Al–Al_2O_3 based device is induced by the Al_2O_3 barrier shell, which requires a larger applied bias to trap electrons from PI into the Al core.[38]

For the device with both NPs (Fig. 2d), it is turned to the first ON state from its initial pristine OFF state at a bias around 1.7 V, which can be maintained until the bias is increased to 3.1 V, the point at which the device is switched to its final ON state. To conclude, the device possesses three states: the pristine OFF state before 1.7 V, the first ON state between 1.7 V and 2.1 V, and the final ON state after 3.1 V. The device cannot be turned OFF from its ON states by applying a negative bias, making it a write-once-read-many type (WORM) memory device. For the three states, the conductivity differs largely, which leads to large current ratios between them (between the OFF state and the first ON state or between the first ON state and the final ON state). Based on the properties of the four devices, we can reliably conclude that the memory properties are indeed from the GD NPs and Al–Al_2O_3 NPs, with the lower-bias one originating from the GD NPs and the higher-bias one originating from the Al–Al_2O_3 NPs.

Afterwards, we measured the electric maintaining ability for every state: we first applied different biases to set the device to the three states, and then fixed the bias at 1 V to test the current fluctuation with time. From the results shown in Fig. 3a, it is seen that the current fluctuates very little in a long duration of 10^4 s. This indicates that the device has a strong retention ability and the three states are all very stable.

The memory mechanism in our device should be originating from carrier tunneling and trapping effects, similar to that reported.[37,38] During the bias scan, carriers are first injected into the GD NPs at a bias around 1.7 V, and then into the Al–Al_2O_3 NPs at a bias around 3.1 V, and are sequentially trapped in the two NP layers. Therefore, there would be different trapped

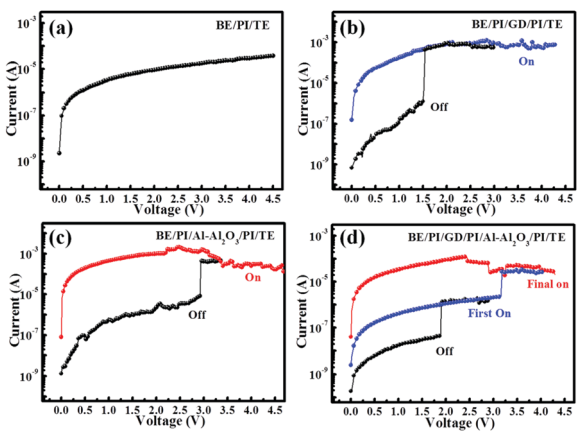

Fig. 2 *I–V* characteristics of the resistive memory devices for (a) a BE/PI/TE structure, (b) a BE/PI/GD/PI/TE structure, (c) a BE/PI/Al–Al_2O_3/PI/TE structure, and (d) a BE/PI/GD/PI/Al–Al_2O_3/PI/TE structure.

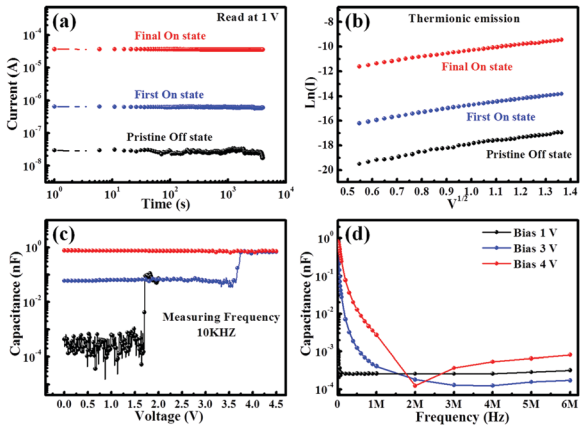

Fig. 3 (a) Retention time test. (b) Results of fitting the *I–V* curves. (c) The capacitance test under voltage sweeping model (measuring frequency 10 KHz). (d) Capacitance test for different bias under the frequency sweeping model.

charges in the device at different states. The *I–V* curves were fitted to investigate the carrier transport mechanism and the tunneling mechanism in the RRAM device using the thermionic emission conduction (TEC) model:[39,40]

$$J \propto T^2 \exp\left[\frac{-q(\phi - \sqrt{qV/4d\pi\varepsilon})}{kT}\right]$$

where ϕ, V, T, ε, d and q represent the barrier height, applied voltage, temperature, insulator dynamic permittivity, thickness of the active layer and charge, respectively. Fig. 3b shows the fitting results for the measured *I–V* curves of the OFF and the ON states with the TEC model. We conclude that the carrier transport in the device at the OFF state and the two ON states can all be dominantly attributed to the TEC process.

The capacitance *versus* voltage is shown in Fig. 3c (including the voltage sweeping mode and the frequency sweeping mode). It is seen that with varying the bias voltage, the capacitance first increases from its initial value to a relatively large value at a bias around 2 V and then to its largest value at a bias around 4 V. The three capacitance values should correspond to the pristine OFF state, the first ON state and the final ON state. The three states are also evident in the frequency sweeping mode (Fig. 3d), when biased under different voltages. Combining the fitting results and the capacitance experiments, we believe that electrons are injected from the Ag electrode into the NPs *via* the TE process and are then trapped in the NPs.

The operation mechanism of the multilevel switching is presented in Fig. 4. Fig. 4a shows the energy level of the pristine state at 0 V without any electrons trapped. During the voltage sweep between 0 V to 1.7 V (Fig. 4b), PI prevents electrons from being injected into the electron traps of the GD NPs and the Al–Al_2O_3 NPs. As a result, the pristine state is stabilized and the device is kept at a high resistance state (HRS). During the first sweep from 0 V to 3 V (Fig. 4c), when the voltage is large enough to overcome the potential barrier formed between the PI and the Ag electrode, electrons are first trapped in the GD NPs, and the device is set to the first ON state. Then, the device is transited from the HRS to an intermediate resistance state (IRS). Owing to the higher Al_2O_3 tunneling barrier shells, electrons cannot be injected into the Al cores. During the second sweep from 0 V to 4 V (Fig. 4d), electrons are injected into the Al cores, and the device is set to its second ON state, the low resistance state (LRS), where it remains.

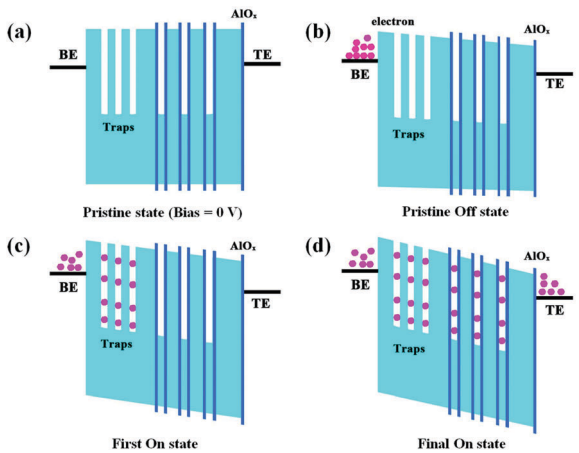

Fig. 4 Switching mechanism of the fabricated multi-state device: (a) pristine state. (b) Pristine OFF state. (c) First ON state. (d) Final ON state.

Conclusions

In summary, we fabricated three-state organic RRAM with high reproducibility and stability by employing the novel carbon material GD and metal/oxide core–shell NPs. The GD NPs produce one ON state and the metal/oxide core–shell NPs produce another ON state. The retention times of the OFF state and the two ON states are all over 10^4 s. On careful analysis based on the *I–V* curve fitting and the *C–V* measurements, we conclude that a carrier tunneling process through the insulator layers and a carrier trapping effect in the two NP layers are responsible for the multilevel memory observations. This study demonstrates that the novel carbon material GD could have great applications in future information storage technologies.

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