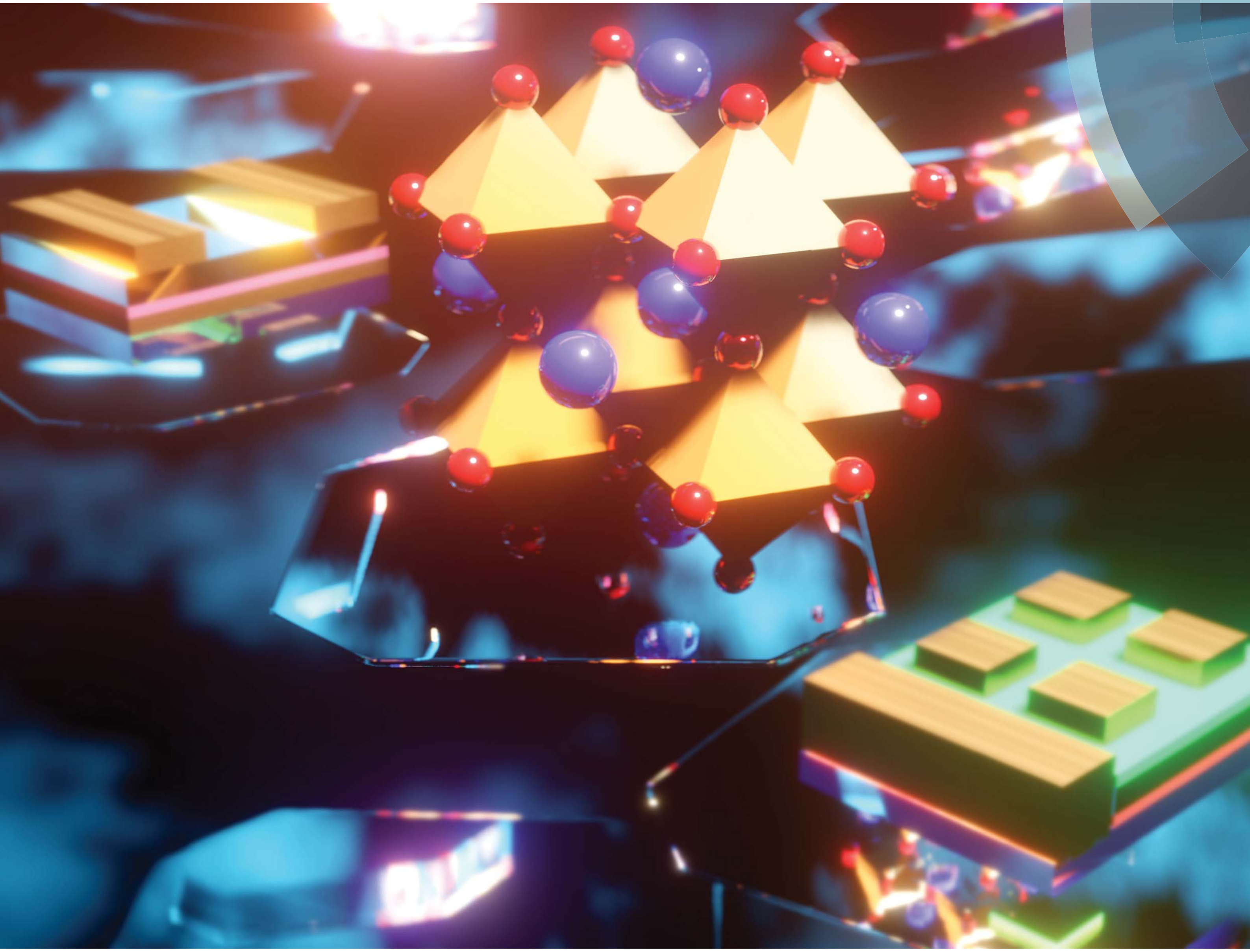
Volume 7 | Number 43 | 21 November 2019 | Pages 24645–25174

Journal of Materials Chemistry A

Materials for energy and sustainability

rsc.li/materials-a



ISSN 2050-7488

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REVIEW ARTICLE
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Journal of
Materials Chemistry A

REVIEW

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Cite this: *J. Mater. Chem. A*, 2019, **7**, 24661

Monocrystalline perovskite wafers/thin films for photovoltaic and transistor applications

Kai Wang,* Congcong Wu,* Yuchen Hou, Dong Yang and Shashank Priya*

High-purity monocrystalline silicon has a long history in the development of photovoltaics; so far, it has dominant applications in modern computers with its profound implementations in transistors and chips. The success of silicon has shown that monocrystalline wafers/thin films of semiconducting materials with superior electronic properties are a good platform for optoelectronic and electronic applications. Recently, the newly emerging semiconducting materials of halide perovskites (HPs) have attracted considerable attention owing to their continuing success in high-efficiency solar cells. The demonstrated optoelectronic properties of HPs indicate that it could be a promising alternative to the silicon-based semiconducting industry. However, the prerequisite of high-efficiency devices is the material accessibility of monocrystalline HPs (mono-HPs), as per the lessons learned from monocrystalline silicon. Current HPs-based technologies, in terms of research areas such as solar cells, photodetectors, light-emitting diodes (LEDs), lasers, and transistors, suffer a bottleneck in manufacturing mono-HP wafers/thin-film materials; hence, exciting results involving mono-HP devices are absent. State-of-the-art optoelectronic HP-based devices are exclusively built using polycrystalline thin films, which are limited in their performance due to issues such as grain-boundary defects, large trap density, and inhomogeneous charge transport. However, these issues can be resolved by utilizing mono-HPs. In this review, we provide in-depth analyses and discussions on the potential of mono-HPs in photovoltaics and transistor applications, and we present the remaining challenges, as well as promising research strategies, to provide a direction for future programs.

Received 12th August 2019
Accepted 13th September 2019

DOI: 10.1039/c9ta08823g

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1. Introduction

Owing to its great abundance and mature infrastructure, silicon-based solar panels/modules have dominated

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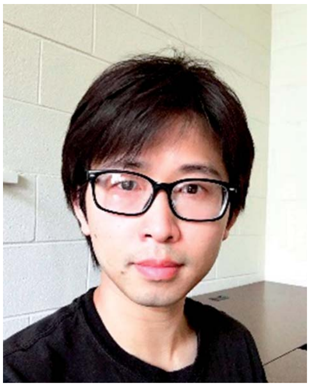

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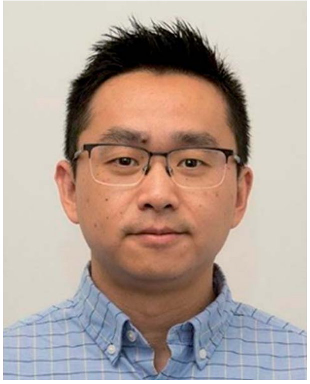

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photovoltaic (PV) technology with over 90% market share.[1,2] High-purity monocrystalline silicon (mono-Si) forms the foundation for transistors,[3] which serve as the basic building blocks of modern computers. Today, silicon-based semiconductor technology is at the heart of the $1 trillion global electronics industry and is vital in many other areas representing the $33 trillion global economy.[4] However, silicon is reaching saturation in many application areas, and it is more obvious in PVs and transistors. Exploring novel semiconductors with superior optoelectronic properties for these platforms is essential for maintaining progress. Recent research progress involving halide perovskites (HPs) has provided a new dimension for fabricating novel semiconductors. The implementation of HPs in PVs has demonstrated solar power conversion efficiency (PCE) of the order of 25%.[5] This PCE magnitude surpasses that of polycrystalline silicon (poly-Si) PVs (22.3%). HPs provide pathways for reaching closer to the Shockley–Queisser limit for single-junction solar cells with theoretical maximum efficiency of 33.7%.[6]

Currently, polycrystalline HP (poly-HP) thin films have been utilized in demonstrating various applications including PVs and transistors. However, the presence of grain boundaries (GBs), large trap density (n_{trap}), and small grain sizes can compromise the electronic properties. In comparison, GB-free monocrystalline hybrid perovskites (mono-HPs) possess ultralong carrier diffusion lengths of up to $\sim$3 mm,[7] which is 4 orders of magnitude higher than their polycrystalline counterparts (*e.g.*, 90 nm in typical poly-HP thin films[8]). The trap density of mono-HPs is of the level of 10^{10} cm^{-3}, which is significantly lower than that of 10^{17}–10^{19} cm^{-3} for poly-HPs[9,10] and even lower than those of typical semiconductor materials such as poly-Si, CdTe/CdS, copper indium gallium selenide (CIGS), and organics (Fig. 1). The existence of these trap states results in the scattering and trapping of charge carriers, thereby reducing charge transport through the Shockley–Read–Hall (SRH) recombination (or the so-called "trap-assisted recombinations"). Even in state-of-the-art perovskite PV devices, SRH recombinations contributes toward major energy loss.[6] Another problem of heat generation caused by hot-carrier thermalization and energy dissipation from SRH recombinations has been often neglected in the literature. This becomes a significant issue in real applications. For example, certain HP materials (*e.g.*, methylammonium lead perovskites) exhibit a high thermal expansion coefficient ($\alpha_{\mathrm{v}} = 1.57 \times 10^{-4}\ \mathrm{K}^{-1}$).[11] Therefore, the temperature-induced phase transition during the day–night cycle could deteriorate the device performance.[12,13] Heat generated from SRH recombinations can be reduced by using mono-HPs, which yield a much lower trap density. In transistor applications, heat generation has also become a prominent issue that degrades the performance and lifetime. In the electronics industry, the heat generated from hundreds of millions of transistors integrated on a single chip could result in reduced power density and degrade the computing power. Thermal cooling has become an important factor in maintaining Moore's law.[14,15] Therefore, the qualification of potential applications in transistors or even on chips, a monocrystalline material is significant as compared to its polycrystalline counterparts. Mono-HP wafer/thin films with ultralow trap density and its GB-independent nature, coupled by its superior optoelectronic properties (such as direct bandgap, excellent charge transport properties, easy material engineering involving large doping space and various compositional modifications, and convenient solution processability, *etc.*), make it a promising platform for constructing next-generation ultrahigh-performance devices.

2. Fundamental merits of mono-HPs

2.1 HP *vs.* typical organic and/or inorganic semiconductors

The "perovskite" structure is named in honor of the Russian mineralogist Lev Perovski who reported the calcium titanium

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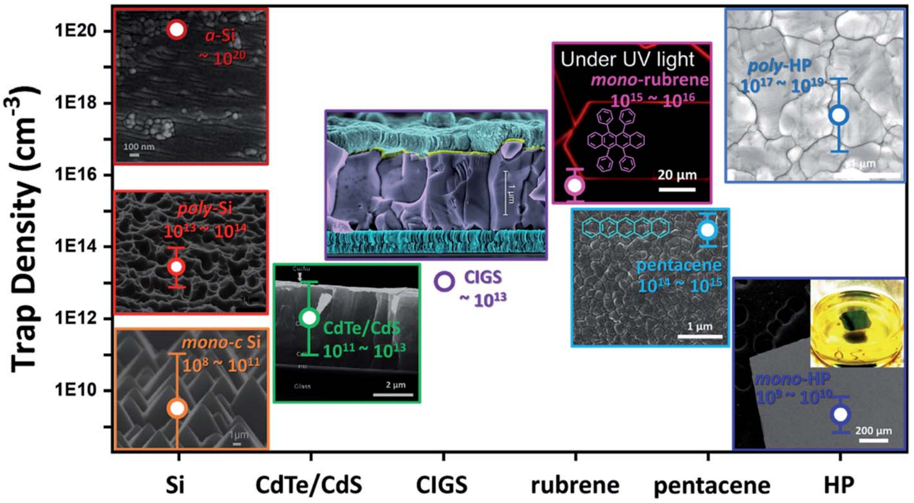


Fig. 1 Comparison of trap densities between typical semiconductors such as amorphous silicon (a-Si),[16] poly-Si,[17] mono-Si,[18] CdTe/CdS,[19] CIGS,[20] mono-rubrene,[21] pentacene,[22] poly-HP,[9] and mono-HP,[23] along with their microscopic images. Credits are given to various sources.[6,24–30] Copyright © 2018 Elsevier Inc. Copyright © 2002 Elsevier Inc. Copyright © 2018 Elsevier Ltd. John Wiley & Sons, 2017, © Copyright 2019 IEEE, © 2007 American Physical Society, © 2002 American Institute of Physics. Copyright © 1999–2019 John Wiley & Sons, Inc. © The Royal Society of Chemistry 2019. Copyright © 2018, Springer Nature. © 2019 Zentrum für Sonnenenergie- und Wasserstoff-Forschung Baden-Württemberg. Copyright © 2017 American Chemical Society. Trans Tech Publications, Ltd. Copyright © 2018, Springer Nature.

oxide ($CaTiO_3$, $^{XII}A^{2+VI}B^{4+}X_3{}^{2-}$) mineral and its unique crystal structure. In the early 1890s, Wells introduced the HP family of lead- and tin-based alkali-metal halides synthesized by Campbell, Walden, and Wheeler.[31] Later, in 1978, Weber synthesized an organic–inorganic hybrid perovskite, namely, $CH_3NH_3PbI_3$ ($MAPbI_3$), by the substitutional doping of alkali metal by an organic cation, namely, methylammonium ($CH_3NH_3{}^+$), at the crystallographic A-site of the perovskite.[32] During the earlier years, the focus of research was on transistor and light-emitting applications, but they were limited by material synthesis and characterization procedures.[33,34] In 2009, Miyasaka's team implemented HP into a dye-sensitized solar cell[35] (DSSC, or "Grätzel cell"). After that, within a decade, HP-based solar cells have exhibited a phenomenal rise in device efficiency from 3% to over 24%.[36] The efficiency of HP-based solar cells is higher than those reported for organic PV (OPV) (16.6%) and inorganic PV such as CdTe (22.1%) and CIGS (22.9%).[36] This high efficiency can be ascribed to the superior optoelectronic properties of HPs. Their direct band structure provides a higher light extinction coefficient ($\eta = 10^5$ cm^{-1} *vs.* 10^3 cm^{-1} of silicon) and small effective mass of electrons and holes (originating from the strong s–p antibonding in the crystal corresponding to $m_h^* = 0.07$ *vs.* 0.29 of silicon). This enables super electrical and bipolar transport (high mobility, μ, up to 10^2 cm^2 V^{-1} s^{-1} *vs.* 10^{-4} cm^2 V^{-1} s^{-1} of organics). Further, HPs exhibit high flexibility in material engineering that allow the tuning of the bandgap (by substitutional doping) to be near the ideal bandgap of 1.34 eV, in accordance with the Shockley–Queisser theory. Detailed discussions on the materials' physics can be found elsewhere.[37] HP is a highly crystalline material that enables the engineering of GBs, trap density, crystal orientation, phase purity, crystal grain size, *etc.* in order to tune the combination of electronic parameters.

2.2 Mono-HPs *vs.* poly-HPs

The record solar cell efficiency (25.2%, KRICT/MIT) of HP PVs involves poly-HP thin films. It is widely agreed that monocrystalline semiconductors have an advantage over polycrystalline semiconductors due to the lower disordered energetic states. Taking mono-HP as an example, due to the elimination of GBs, the trap density can be reduced to $n_{trap} = 10^9$ cm^{-3} (*vs.* 10^{17} cm^{-3} in poly-HPs, as shown in Fig. 1),[9,23] carrier mobility can be increased to $\mu = 200$ cm^2 V^{-1} s^{-1} (*vs.* 0.4–40 cm^2 V^{-1} s^{-1} in poly-HPs),[38,39] carrier lifetime can be increased to $\tau = 500$ ms (*vs.* 4.5–1000 ns in poly-HPs),[40] and carrier diffusion length can be increased to $L_D = 3$ mm (*vs.* 90 nm in poly-HPs).[7,8] These features mitigate parasitic issues in solar cell devices, such as photocurrent hysteresis, ion migration, and degradation inherent in typical polycrystalline devices. Overall, these features have raised the question whether a mono-HP PV can exhibit better device performance than that of its polycrystalline counterparts or not. A positive answer for mono-Si PV gives us a hint of optimism since mono-Si PVs display record PCE of 26.7%, in contrast to that of poly-Si PVs (22.3%).[6] Taking inspiration from mono-Si PVs and building upon the achievements of poly-HPs, we expect that mono-HP PVs can create opportunities to further enhancing the efficiency. Recent discoveries involving ferroelectric electron–hole channels,[41,42] highly conductive layered-edge states,[43] slower hot-carrier cooling,[44] and photon recycling processes[45] have inspired proof-of-concept mono-HP devices with improved PCEs. To understand this, the slow hot-carrier cooling in mono-HPs has been predicted to result in a potential PCE value of 66%,[44] which is far higher than the Shockley–Queisser limit of 33.7% for typical single-junction PVs.

2.3 Mono-HP membrane (mono-HP wafer/thin film) *vs.* mono-HP bulk

During the past few years, mono-HP bulk materials with dimensions ranging from a few millimeters to several inches have been grown and applied in optoelectronic applications such as PVs,[46] detectors,[47] and light emitters.[48] However, typical bulk single crystals have larger geometric dimensions as compared to their maximum charge diffusion length. For example, for sample handling and actual implementation, a bulk mono-HP needs to have a dimension of the order of centimeters, which is significantly larger than its maximum carrier diffusion length (*e.g.*, 175 μm for $MAPbI_3$ (ref. 49)). In most of the cases, the depletion width also needs to be taken into consideration to ensure higher charge collection efficiencies.[50] Hence, in the case of bulk mono-HPs-based PVs, the photogenerated charge carriers traveling beyond the maximum diffusion length and/or the depletion width typically contribute toward energy loss *via* the recombination process. To minimize these recombination losses, reducing the thickness of mono-HPs to comply with the diffusion and/or depletion limit is imperative. Consequently, mono-HP wafers/thin films with suitable thickness can provide a solution to rectify efficiency losses. As shown in Fig. 2, mono-HP wafers/thin films are expected to deliver better performance in PVs and transistors.

3. Techniques for growing mono-HP wafers/thin films

Although the advantages of mono-HP wafers/thin films have been recognized, the realization of product-oriented mono-HP wafers/thin films that meets device requirements remains to be achieved. These requirements include large aspect ratio (*i.e.*, large basal area but small thickness), smooth surface, low surface trap density, controllable crystal facet orientation, and good compatibility with the target substrate. In terms of device construction, both wafers and thin films could be utilized, as solar cells and transistors can be either built from free-standing mono-HP wafers by coating functional layers on both the sides (analogous to the manufacturing of mono-Si PVs) or from mono-HP thin films that are grown on FTO and/or ITO electrodes followed by metal electrode deposition. Several methods have been proposed in the literature to provide mono-HP wafers/thin films. These include the (i) floating method, (ii) space-limited growth method, (iii) vapor-phase epitaxy (VPE), and (iv) bulk crystal dicing. In this section, we will discuss these techniques that can be used for growing mono-HP wafers/thin films emphasizing on the crystallization mechanisms and growth processes.

3.1 Floating method

The driving force for the precipitation of a solid phase from a supersaturated solution is quantified as the chemical potential difference ($\Delta\mu$) of a molecule between the solution and bulk crystal phase:

$$\Delta\mu = \mu_s - \mu_c \tag{3.1}$$

where μ_s and μ_c are the chemical potential of a molecule in solution and in the bulk crystal, respectively. Eqn (3.1) can also be thermodynamically expressed as

$$\Delta\mu = kT \ln S \tag{3.2}$$

where *k*, *T*, and *S* are the Boltzmann constant, absolute temperature, and supersaturation ratio, respectively. The initiation of supersaturation can be achieved through temperature adjustment (cooling), concentration changes (concentrating), or by altering the solution activity coefficients as those in the solvent/antisolvent method (denoted by purple dashed arrow in Fig. 3a) according to the temperature–composition phase behavior shown in Fig. 3a. Evidently, the solubility curve represents thermodynamic equilibrium between the phases. For most perovskite systems with compositions and temperatures below the solubility curve, a stable "unsaturated zone" (blue region in Fig. 3a) exists. Typical systems have a positive

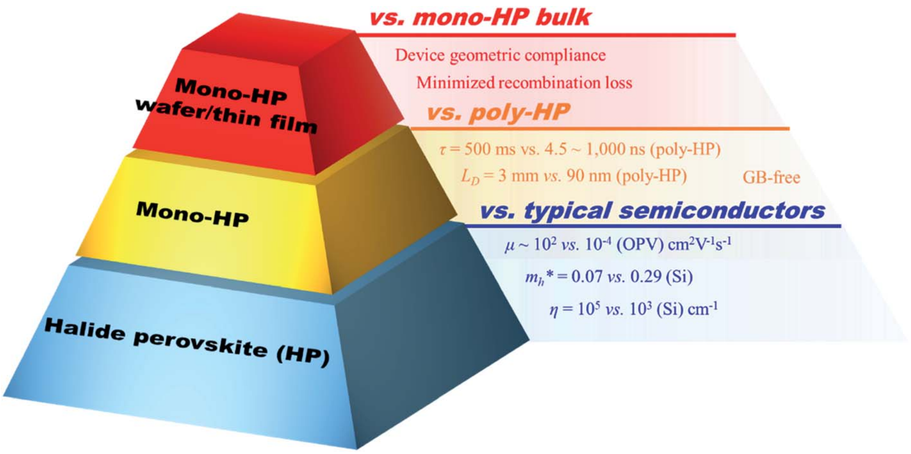


Fig. 2 A "Mesoamerican pyramid" showing the relationship between mono-HP wafers/thin films, mono-HPs, and HPs, as well as their comparison with mono-HP bulk, poly-HPs, and other typical semiconductors.

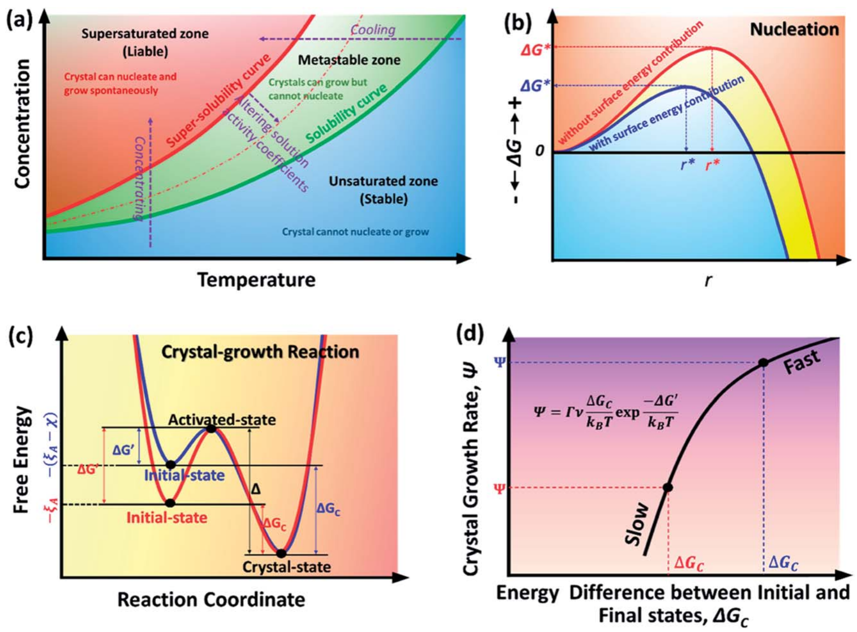


Fig. 3 Crystallization theory. (a) Solubility curve and metastable zone plotted against temperature and concentration. (b) Total free energy *versus* cluster size, (c) reaction coordinate diagram, and (d) crystal growth rate *versus* energy difference between the initial and crystal states, showing that the surface tensile stress contributes toward both lower nucleation barrier and faster crystal growth rate.

correlation between solubility and temperature; hence, reducing the temperature of a saturated solution can trigger crystallization. However, some HP solutions have an "inverse" dependence between solubility and temperature. For example, the solubility of $MAPbI_3$ in a GBL solution increases with temperature.[51] Here, a higher temperature is required to induce supersaturation. In any case, beyond this solubility limit, the liquid might not be in thermodynamic equilibrium with respect to the formation of its solid phase, which is termed as the "metastable zone" (green region in Fig. 3a). In this region, spontaneous nucleation is difficult to occur, but crystal growth is easy, implying that this is the perfect region for growing a larger crystal from a smaller one. Typically, in order to initiate the formation of a solid phase, heterogeneous nucleation sites need to be introduced. Beyond the boundary of the "metastable zone," these nucleation seeds are no longer required, and the region becomes the "supersaturated zone" (red region in Fig. 3a), which is neither stable nor in equilibrium; therefore, it is subject to spontaneous nucleation and rapid crystal growth.

Initiating nucleation requires overcoming the free energy barrier (ΔG_T), which is set by the free energy difference between the system in its final and initial states ($\Delta\mu$) plus a surface-tension-related term ($4\pi r^2\sigma$):[52]

$$\Delta G_T = -\frac{4}{3}\pi\frac{r^3}{V}\Delta\mu + 4\pi r^2\sigma \tag{3.3}$$

where r, σ, and V are the radius of the nucleus, surface free energy, and volume of each molecule, respectively. Fig. 3b shows the ΔG_T value as a function of r. Evidently, this relation elucidates the manner in which the function reaches the maximum, representing the fact that the energy barrier (ΔG^*) should be overcome to initiate nucleation. The magnitude of ΔG_T heavily depends on the surface free energy (σ), so any process that could change this value would have a significant effect on the nucleation process. A classic example is the introduction of foreign seeds; this has been utilized in the "Czochralski method".[53] In the case of HPs, the nucleation can first occur at the "solution/substrate" interface as the presence of a foreign substrate can decrease the surface energy σ, reducing ΔG_T by a factor of $f(\theta)$ according to the following equation:[52]

$$\Delta G_{\text{solution/substrate}} = \Delta G_{\text{hetero}} = \Delta G_{\text{homo}} f(\theta) \tag{3.4}$$

$$f(\theta) = \frac{2 - 3\cos\theta + \cos^3\theta}{4} \in [0,\ 1] \tag{3.5}$$

where θ is the contact angle of the solution on an alien substrate surface. A wetting substrate has a higher probability of inducing nucleation as it has a smaller contact angle and resultant smaller value of $f(\theta)$ is closer to 0, which renders a lower energy barrier (ΔG^*). The "solution/air" interface is often neglected, where the existence of surface tension can reduce the energy barrier. In our recent study,[54] we have developed a simplified model to illustrate the surface energy contribution to facilitate nucleation at the water–air interface. The analysis considered to involve a type of precursor molecule (A) that can exist in the form of (i) free precursor molecule "A," (ii) "A-cluster" nucleus, and (iii) solvated complex "$A - jS$," where A is intermolecularly bonded with j solvent molecules (S) having complex binding energy E_C. We derived the free energy difference expressions for nucleation in either a bulk solution or at the "solution/air" interface. In contrast to the bulk solution, the molecules at the "solution/air" interface experience extra tensile elastic stress (surface energy contribution) that increases the energy of the precursor molecules by χ (>0) and results in a reduced energy barrier by contributing χ to the denominator, as shown in the following equation:

$$\Delta G_{\mathrm{solution/air}} = \frac{16}{3}\pi\sigma^3 \times \left(\xi - E_{\mathrm{C}} - \xi_{\mathrm{A}} + \chi + k_{\mathrm{B}}T\ln\frac{1}{\frac{{M_{\mathrm{S}}}^j}{M_{\mathrm{A}}} - j^2{M_{\mathrm{S}}}^{j-1}}\right)^{-2} \tag{3.6}$$

where ξ (>0) is the cohesive energy of the precursor molecules in the cluster, ξ_{A} (>0) is the energy of the precursor molecules, σ is the surface tension coefficient, k_{B} is the Boltzmann constant, T is the temperature, and M_{S} and M_{A} are the total molar concentrations of the solvent and precursor molecules, respectively. Fig. 3b shows a comparison of the free energy differences with and without the tensile elastic stress. Clearly, at the "solution/air" interface, there is a contribution from the surface energy/tensile elastic stress toward reducing the energy barrier (ΔG^*), which enhances the probability of nucleation (blue line in Fig. 3b).

In terms of crystal growth, particularly for growing a large single crystal, the crystal growth needs to be controlled in the "metastable zone" (Fig. 3a) to eliminate other nuclei seeds and hence only one nucleus grows into a larger single crystal. In the solution, the crystal can grow in any direction to achieve larger dimensions. In order to confine the resultant crystal into having wafer/thin film geometry, a strategy relying on the surface energy has been developed.[54,55] Fundamentally, the crystal growth rate (Ψ) can be determined by the rate of competition between the molecular attachment and detachment:[54]

$$\Psi = \Gamma\nu\frac{\Delta G_{\mathrm{C}}}{k_{\mathrm{B}}T}\exp\frac{-\Delta G'}{k_{\mathrm{B}}T} \tag{3.7}$$

$$\Delta G' + \Delta G_{\mathrm{C}} = \varDelta \tag{3.8}$$

$$\Delta G' = G_{\mathrm{a}} - G_{\mathrm{i}} \tag{3.8a}$$

$$\Delta G_{\mathrm{C}} = G_{\mathrm{f}} - G_{\mathrm{i}} \tag{3.8b}$$

$$\varDelta = G_{\mathrm{f}} - G_{\mathrm{a}} \tag{3.8c}$$

where Γ is a geometric factor; ν is the attempt frequency; and $\Delta G'$, ΔG_{C}, and $\varDelta$ are the free energy differences between the initial (G_{i}) and activated (G_{a}), between initial (G_{i}) and final (G_{f}), and between activated (G_{a}) and final states (G_{f}), respectively, as shown in Fig. 3c. As compared to the inner solution, at the "solution/air" interface, the additional surface tensile stress contributes toward higher energy in the initial state (blue line in Fig. 3c). Therefore, according to eqn (3.7), a larger crystal growth rate (Ψ) can be achieved. Fig. 3d shows the relationship between the crystal growth rate (Ψ) and free energy difference between the initial and final states (ΔG_{C}). Larger ΔG_{C} renders higher Ψ. As a result, faster lateral growth along the solution/air interface against vertical growth is expected in the inner solution.

Relying on this mechanism, mono-HP wafers/thin films can be fabricated by using the floating method. Several groups have fabricated free-standing mono-HP wafers by exploiting the solution/air interface. Fig. 4a shows an example of mono-HP wafer growths for two-dimensional (2D), quasi-2D, and three-dimensional (3D) perovskites of $\mathrm{BA_2MA_{n-1}Pb_nI_{3n+1}}$, where n = 1 (2D), 2, 3, … (quasi-2D), ∞ (3D).[54] Here, BA is *n*-butylammonium ($\mathrm{CH_3(CH_2)_3NH_3^+}$) and MA is methylammonium ($\mathrm{CH_3NH_3^+}$). It should be noted that the $\mathrm{BA^+}$ cation is an amphiphilic long molecule comprising a hydrophilic ammonium cation head and a hydrophobic alkyl chain. Such an amphiphilic molecule can align itself with a head-down pattern at the water–air interface. Further, the ammonium cation head can act as a template for the molecular assembly underneath to direct facet orientation during crystal growth. By controlling the chemical composition, *i.e.*, the ratio between BA and MA in the solution, the final crystal can be tuned from a 2D multi-quantum-well (MQW) structure to a 3D perovskite.[54] Similarly, for other 2D perovskite systems such as $\mathrm{(PEA)_2PbI_4}$ (PEA is phenylethylammonium, *i.e.*, $\mathrm{C_6H_5(CH_2)_2NH_3^+}$)), free-standing single crystals can be obtained from the floating method. From Fig. 4b, it is evident that Liu *et al.* reported single-crystal synthesis floating at the solution surface.[56] By tuning the temperature, the aspect ratio can be controlled, too. Other 3D perovskite materials, such as $\mathrm{MAPbBr_3}$, $\mathrm{MAPbI_3}$, and $\mathrm{MASnBr_3}$, can also be fabricated by using a similar method. Fig. 4c–f show the corresponding 3D mono-HP wafers/thin films obtained from different groups.[55,57]

Notably, the advantages of the floating method include the ability to control the crystal facets, as the spontaneous alignment of an amphiphilic nanotemplate can direct the assembly in a predictive pattern. Understanding the operating mechanism of a surfactant monolayer that adapts to the perovskite precursive ions at the solution/air interface and guides the epitaxial growth of nanosheets can bring more insights into this field. Similar attempts have been successfully made in growing ZnO nanosheets, which is also termed as the adaptive ionic layer epitaxy (AILE) method.[58] In addition, scaling up the mono-HP wafer by enlarging the area of the solution surface may boost the development of mono-HP-based applications. Coincidently, an analogical methodology called the "float glass process" for manufacturing flat glasses in the industry has been developed and widely applied. Actively utilizing these learnings from the related fields of glass manufacturing may further accelerate the development of mono-HP-wafers-/thin-films-based optoelectronics.

3.2 Space-limited growth method

In order to obtain a flat single crystal with a large aspect ratio, the floating method takes the advantage of "energy confinement", where the surface energy contribution confines the crystal growth along the solution/air interface. A more straightforward way is to use "space confinement", or the "space-limited growth method." In this case, the crystal growth occurs in a geometrically designed "container" that has a flat chamber (Fig. 5a). The technologies for typical bulk

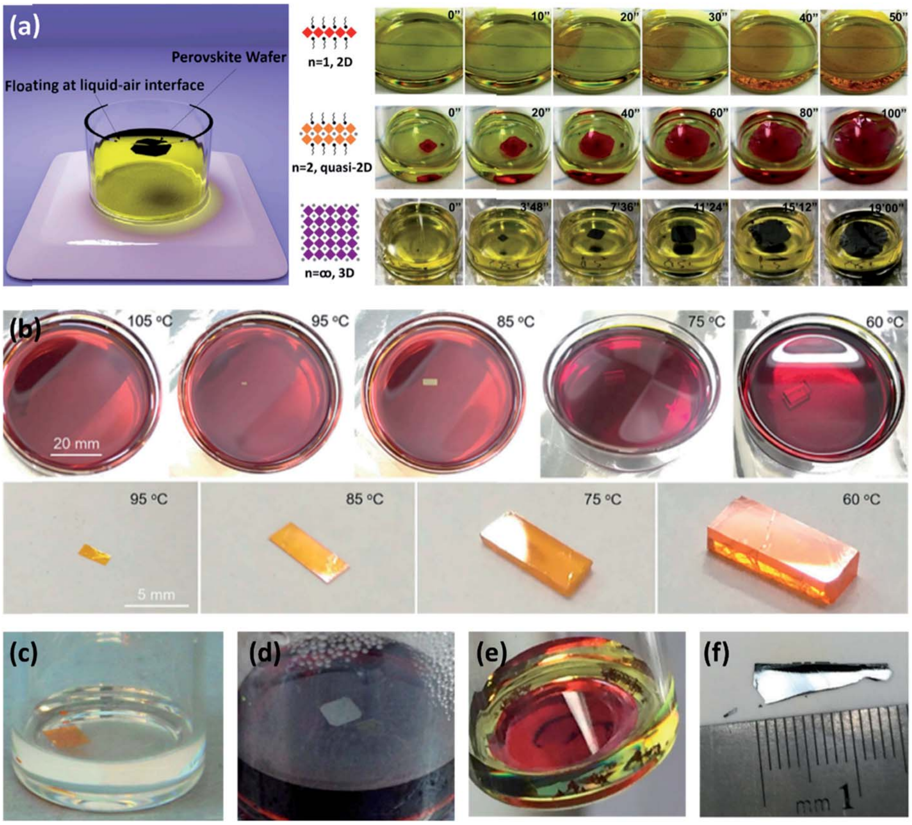


Fig. 4 Various mono-HP wafers/thin films synthesized using the floating method. (a) $BA_2MA_{n-1}Pb_nI_{3n+1}$, where $n = 1, 2, 3, \ldots, \infty$, adapted from reference.[6,54] Copyright © 2018 Elsevier Inc. Copyright © 2018 American Chemical Society. (b) $(PEA)_2PbI_4$.[56] Copyright © 2019 Copyright Clearance Center, Inc. (c) $MAPbBr_3$, (d) $MAPbI_3$, and (e) $MASnBr_3$.[55] Copyright © 2017 American Chemical Society (f) photograph of 1.5 cm-long $MAPbI_3$ single-crystal piece of wafer.[57] Copyright © 1999–2019 John Wiley & Sons, Inc.

crystallization such as solution temperature lowering,[59] inverse temperature crystallization,[51,60] antisolvent vapor-assisted crystallization,[61] and melt crystallization[62,63] can be easily adopted for the space-limited growth method. The flexibility in designing a "container" and accommodating it into a narrow crevice helps in achieving flat mono-HP wafers/thin films with large aspect ratios. For example, by shrinking the gap between two substrates, the thickness of the membrane can be tuned from 13 nm to 4.5 mm.[64] Chen *et al.* employed two clean flat substrates clipped together, which were subsequently vertically dipped in a perovskite-saturated solution.[64] The capillary pressure drives the solution such that it fills the gap between the substrates. The gap can be modulated by the clipping force. Upon heating the bottom precursor solution to reach the saturated state, the top solution can be tuned into a supersaturated state through the top-seeded solution growth (TSSG) method.[49] Hence, the crystal can be grown from a slit (Fig. 5b). Liu *et al.* also demonstrated the early $MAPbI_3$-single-crystal wafer (thickness: 150 μm) by fabricating an ultrathin-geometry-defined dynamic-flow reaction system.[65] Rao *et al.*[66] demonstrated a mono-HP thin film of $CH_3NH_3PbBr_3$ on an FTO glass substrate with a large area of 120 cm^2 and controllable thickness of 100–800 mm. To reduce this thickness, an optimized module with a smaller laminar distance of 16 μm and mass-transport circulating flow to supply the precursors has been developed. This can render a mono-HP thin film with a larger aspect ratio.[67] As the nucleation process takes place in a narrow channel, the adhesion of precursor molecules on the substrate surface can lead to unbalanced local concentrations, inducing multiple nuclei and transforming the structure into a polycrystalline film.[68] Chen *et al.* introduced hydrophobic coaters (*e.g.*, PTAA) on the substrate to facilitate the microflow and obtained millimeter-sized mono-HP thin films of $MAPbI_3$ and $MAPbBr_3$ with thicknesses in the range of tens of micrometers.[68]

As mentioned above, the surface energy can have a huge impact on the nucleation barrier. Yang *et al.*[69] employed substrates that already underwent surface treatment to modulate the energy barrier. Briefly, hydrophobically treated silicon and hydrophilically treated ITO glass were used as the two substrates for crystal growth. The nucleation energy barrier was reduced on the ITO glass for supporting the selective growth of $MAPbBr_3$ mono-HP thin films. A thickness of 365 nm and lateral size of >600 nm were obtained in this way. Normally, the solubility increases with the temperature. In certain perovskite solution systems, such as $MAPbI_3$ in GBL, the solubility reaches the maximum at 60 °C and further increasing the temperature can significantly decrease the solubility.[70] Relying on this

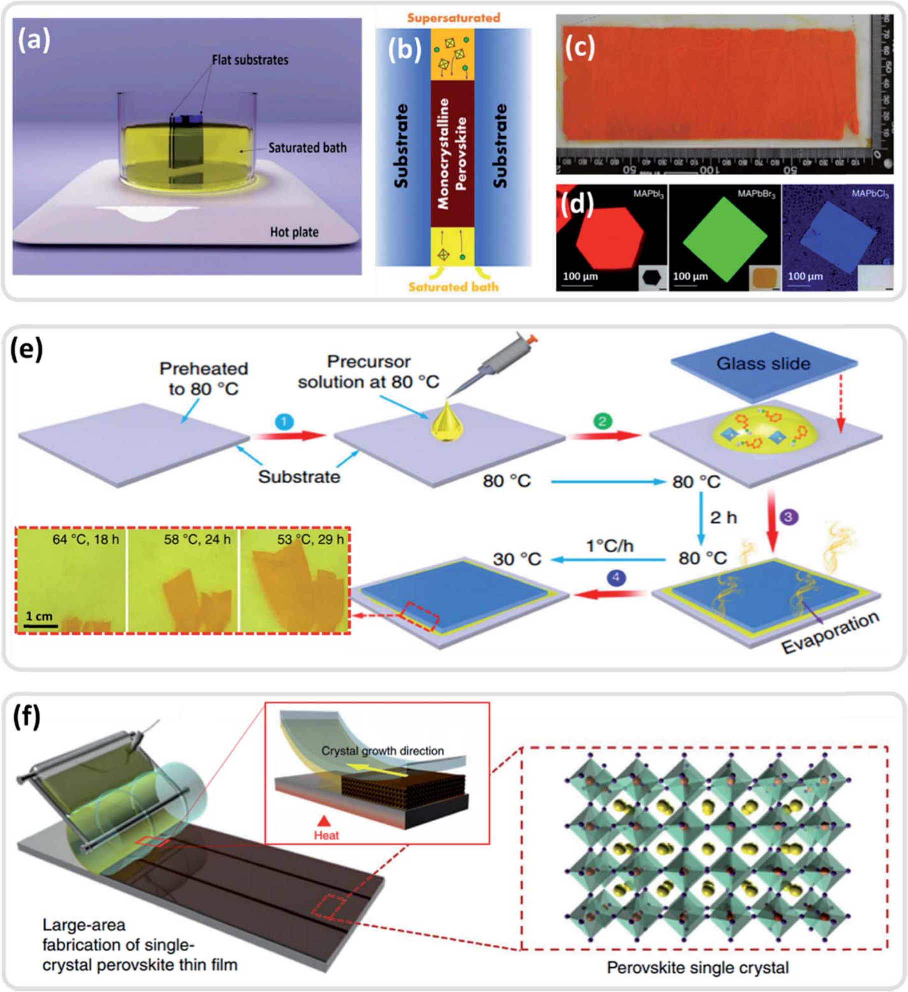


Fig. 5 Examples of space-limited growth methods. (a) Basic experimental setup for the space-limited growth method. (b) Schematic illustration of a spatially confined crystal grown in a narrow crevice constructed by two flat substrates.[6] Copyright © 2018 Elsevier Inc. (c) Photograph of a $MAPbBr_3$ crystal thin film grown from this method, with a thickness of 0.4 mm and area of 120 cm^2.[78] Copyright © 1999–2019 John Wiley & Sons, Inc. (d) Fluorescence microscopy images of $MAPbI_3$, $MAPbBr_3$, and $MAPbCl_3$ single-crystal flakes grown by using the space-limited growth method.[71] Copyright © 2018, Springer Nature. (e) A schematic illustration of the capping method, coupled with the photographs of the resultant single-crystal flakes.[76] Copyright © 2018, Springer Nature. (f) Schematic of the GC-LCG method.[77] Copyright © 2017, Springer Nature.

phenomenon, inverse temperature crystallization[51,60] has been applied in growing bulk crystals. Introducing the inverse temperature crystallization[51,60] into the space-limited growth method can simplify the experimental procedure, as nucleation can be triggered only by elevating the solution temperature. Yu *et al.*[71] showed (Fig. 5d) that the space-limited growth method coupled with inverse temperature crystallization yields the successful synthesis of mono-HP thin films of $MAPbX_3$, $X = Cl$, Br, or I, with tunable lateral sizes ranging from micrometers to millimeters. Yue *et al.*[72] also applied a similar strategy for growing $MAPbI_3$. They demonstrated that unlike $MAPbBr_3$, $MAPbI_3$ is more difficult to be synthesized through the space-limited growth method due to the distinct solubilities of MAI and PbI_2 in GBL. A $MAPbI_3$ seed crystal is then employed to bypass the nucleation barrier and obtain a mono-HP thin film of $MAPbI_3$ with thicknesses of 50 μm and lateral dimensions of up to 2 mm.[72]

Instead of immersing the two-substrate chamber into the saturated solution in Fig. 5a, the derivatives of the space-limited growth method could take advantage of the evaporation of solvent molecules to concentrate the solution, thereby reaching the supersaturation zone, as shown in Fig. 3a. Therefore, the method of "cast capping" has been attempted in which the wet saturated solution is capped by a coverslip followed by the evaporation of solvents in order to grow the mono-HP thin film.[68,73,74] Yanagi's group has reported this method to grow millimeter-sized mono-HP thin films for laser and light-emitting diode (LED) applications.[73,75] It should be noted that in order to optimize the crystallization process, several experimental conditions such as environmental atmosphere, solvent evaporation rate, temperature, and saturated vapor pressure need to be tuned during the process. A successful example is the growth of $(PEA)_2PbI_4$ mono-HP thin film by Liu *et al.*[76] Fig. 5e shows an illustration of the experimental procedure. Briefly, one drop of the prepared precursor solution [PbI_2 : PEA (1 : 2 molar ratio) was dissolved in GBL at 80 °C at a concentration of 2.12 M] is pipetted onto a glass substrate preheated to 80 °C. A second glass slide with a smaller size is then placed onto the solution drop that pushes the solution to evenly spread in the channel. After maintaining the system at 80 °C in an enclosed oven, the evaporation of the solvent from the edge can concentrate the solution into an oversaturated zone and successively lead to nucleation and crystal growth. With an optimal temperature ramp rate, the resultant $(PEA)_2PbI_4$ mono-HP thin film exhibited a size of >73 × 35 mm^2 and a thickness of 0.6 μm; this was the first time that a large mono-HP thin film was fabricated with an area exceeding 2500 mm^2 but a thickness lower than 10 μm.[76]

Another innovation building upon the space-limited growth method can be obtained in combination with the roll-to-roll printing technology. Lee *et al.*[77] demonstrated the wafer-scale patterned mono-HP thin film by using the "geometrically confined lateral crystal growth (GC-LCG)" method. Fig. 5f shows the schematic of the manufacturing setup. A spatially limited microchamber was constructed for crystal growth with a cylindrical metal roller wrapped with polydimethylsiloxane (PDMS) mold. It exhibited a periodic array of wide and shallow channels with a width of 10 mm, depth of 200 nm, and a narrow distance of 400 nm between the channels. Initially, a roller mounted with an ink supplier, which is filled with a perovskite precursor ink, is placed in contact with the preheated substrate. At the open end of the channel, crystallization occurs instantly when the ink comes into contact with the hot substrate due to rapid solvent evaporation. With an optimal rolling speed of the mold, the seed crystals at the end can direct crystal growth from the solution near the end. The crystal growth in the vertical direction is confined within the mold, and the lateral crystal growth is also regulated by the channel; hence, misaligned growth can be avoided. Patterned (10 mm-wide and 200 nm-thick strips with 400 nm-wide spacing) mono-HP thin films (3 × 3 in^2) on the SiO_2 substrate could obtained using this process. The striking feature of this technology is the fast and large-scale production, as well as the ability to control the crystal growth direction.[77]

The "space-limited growth method" offers a straightforward way for growing mono-HP thin films using these strategies for bulk crystals. Nevertheless, several open questions need to be resolved before moving onto the next stage: (i) the first difficulty lies in the appropriate construction of an optimal container with a large aspect ratio on the inch scale in a basal plane but on the nanometer scale in height with satisfactory inner surface homogeneity, as the surface morphology of the single-crystal membrane grown inside the container is largely dependent on the nanostructures of the container surface; (ii) the post-processing of exfoliating the crystal from the container remains to be another challenge, since the physical release can inevitably induce structural damage during the mechanical cleavage between perovskite and container wall; (iii) careful facet growth control needs to be reconsidered as the charge behavior may anisotropically depend on the reciprocal lattice orientation, particularly in lower-dimensional perovskites, whereas the "space-limited growth method" cannot govern facet orientation due to random nucleation inside the narrow space.

3.3 VPE

VPE is a ubiquitously powerful technique for growing IIIA-VA semiconductors such as GaAs, GaP, InP, GaAsP, and InGaAsP. Fig. 6a shows a simple setup of the VPE method, where the vapor-phase precursors are transported into the reaction chamber to trigger and directly grow a single-crystal thin film on a susceptor. The VPE has been documented previously to be a successful technique for growing p-type GaN for blue LEDs.[79] This method can provide high phase purity and yield ultrathin single-crystal thin films with thicknesses at the monolayer level.[80] Nevertheless, the major challenges are difficulties in finding a compatible substrate whose lattice constant and expansion coefficient could match well with that of the objective materials. Meanwhile, to vaporize the precursor molecules, temperature control and material stability—particularly for organic ammonia that has a lower thermal stability—also need to be taken into consideration. So far, there has been a hindrance in applying this method to grow organic–inorganic mono-HP thin films.

It was not until recently that Shi's group achieved VPE-assisted mono-HP thin-film growth on a van der Waals (VDW) substrate.[80] As shown in Fig. 6b, they compared the atomistic nucleation between a conventional and VDW epitaxy process. For the conventional case, the strong chemical bond between the adatom and the substrate leads to a very small critical nucleus (down to a single atom) and a large diffusion barrier (E_d). However, for the VDW case, the inert substrate is free from dangling bonds and only small dipole moments are present. Therefore, the adsorption energy (E_{ad}) is small in this case, which leads to a more difficult nucleation process since more "simultaneous" collisions of adatoms on the substrate are needed. In addition, the higher-energy VDW bonding state makes the diffusion barrier (E_d) extremely low according to several simulations.[81] By quantifying the lifetime of adatoms (τ_a) during the nucleation process by

$$\tau_a = \nu^{-1}\exp\left(\frac{E_{ad}}{kT}\right) \tag{3.9}$$

where ν is the vibration frequency and k is the Boltzmann constant, and by performing an analysis using the Walton's model, the nucleation barrier (ΔG^*) can be calculated by using either the conventional or VDW epitaxy process. For HPs with extremely low cohesive energy and strong ionic character, a significant proportion of large-scale monolayer growth under proper growth conditions is expected (Fig. 6c). They obtained $MAPbCl_3$ mono-HPs with large-scale ultrathin sheets and high crystalline phase purity (Fig. 6d and e).[80] By adjusting the substrate and target material in terms of lattice constant, mono-HP thin films of $CsSnBr_3$ and $CsPbBr_3$ have been grown on NaCl substrates. Fig. 6f–h show an illustration of the heterostructure and the corresponding SEM images. The obtained mono-HP thin films exhibit smooth surfaces with uniform and

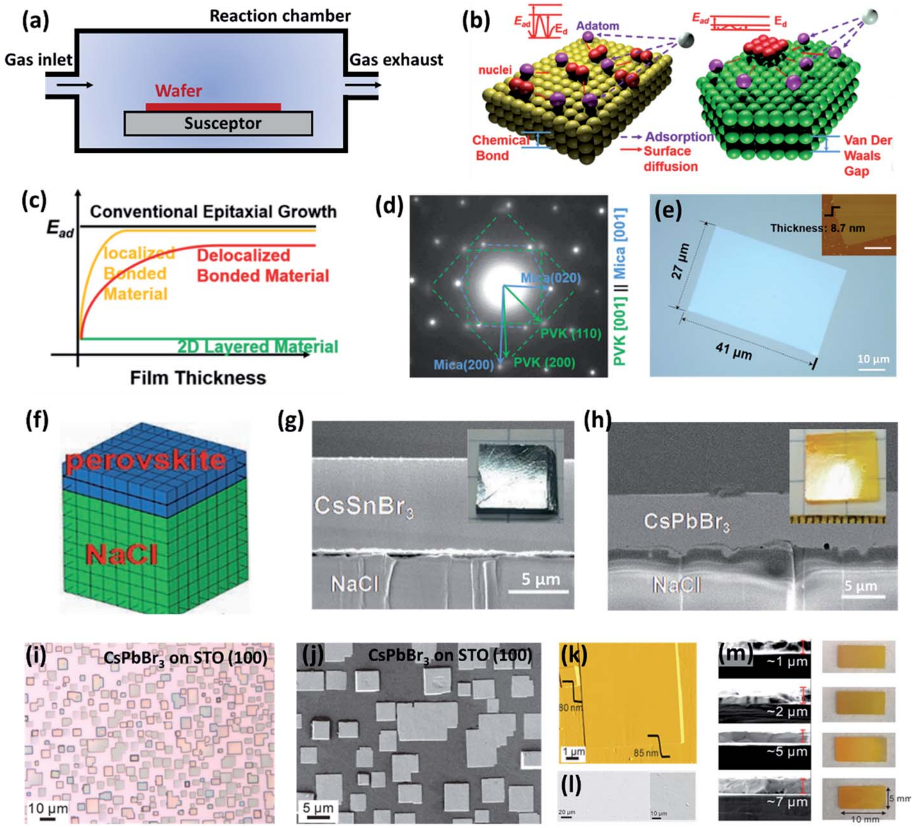


Fig. 6 VPE method for growing mono-HP thin films. (a) A simple VPE reactor prototype. (b) Schematic drawing showing the different atomistic processes on a conventional (yellow) and VDW (green) substrate in terms of adsorption energy (E_{ad}), diffusion barrier (E_d), and nuclei sizes. (c) Schematic drawing of the manner in which E_{ad} changes with thickness for three types of materials. (d) Electron diffraction pattern of mono-HPs on a mica substrate. (e) Optical image of an individual large-scale ultrathin mono-HP sheet (inset showing the atomic force microscopy measurement of the film thickness).[80] Copyright © 2015 American Chemical Society. (f) Illustration of the heterostructure of a mono-HP thin film grown on a NaCl substrate. SEM images of (g) $CsSnBr_3$ and (h) $CsPbBr_3$ mono-HP thin films on a NaCl substrate, coupled with the photograph of a real sample.[82] Copyright © 1999–2019 John Wiley & Sons, Inc. (i) Optical microscopy and (j) SEM image of $CsPbBr_3$ nanoplates grown on a STO (100) substrate. (k) Representative AFM images and (l) top-down SEM image of $CsPbBr_3$ mono-HP thin film (thickness: 7 μm). (m) Cross-sectional SEM images and photographs of $CsPbBr_3$ mono-HP films with varying thicknesses of 1, 2, 5, and 7 μm.[83] Copyright © 2017 American Chemical Society.

adjustable thicknesses from ~200 nm to ~7 mm.[82] Moreover, $SrTiO_3$ (STO) can also act as a good susceptor substrate, due to a the low lattice mismatch factor with $CsPbBr_3$.[83] By increasing the reaction temperature to 450 °C, atomic diffusion is accelerated to foster nucleation and crystal growth. Large-area continuous mono-HP thin films of $CsSnBr_3$ with good single crystallinity and orientation (Fig. 6i and j) can be readily grown on the (100) facet of STO substrates, with adjustable thicknesses from 80 nm (Fig. 6k) to 7 μm (**Fig. 6m**). In particular, this method can be specially used for synthesizing all-inorganic perovskite materials; however, for organic–inorganic perovskites (such as $MAPbI_3$ and $FAPbI_3$), the high reaction temperature (over 400 °C) can significantly degrade the organic moieties.

3.4 Bulk-crystal slicing

Earlier, we discussed the current technologies for growing mono-HP wafers/thin films starting from a solution. The geometric features such as flatness, large basal size, and small thickness are limited either by the energetics barriers (surface energy in the floating method; adhesion and diffusion energies in the VPE method) or spatial objects (narrow channel in the space-limited growth method). On the other hand, industrial mono-Si wafer manufacturing either for solar panel or chip industry applications can be exclusively based on the bulk-crystal slicing technology, which follows a top-down procedure. Fig. 7a shows the simplified manufacturing flowchart comprising a mono-Si ingot pulling process and a Si-wafer-forming process. Briefly, raw materials (such as silica) are smelted and refined into polycrystalline silicon, which is further manufactured into a monocrystalline silicon ingot through the Czochralski method that uses chunks of virgin polycrystalline silicon. These chunks are melted and placed in a quartz crucible along with small quantities of dopants (*e.g.*, boron for p-type doping; phosphorus, arsenic, and antimony for n-type doping). After heating to ~1420 °C (above the melting temperature of Si), a seed is put on the top to nucleate the Si and direct the orientation of the crystal. By modulating the pulling speed,

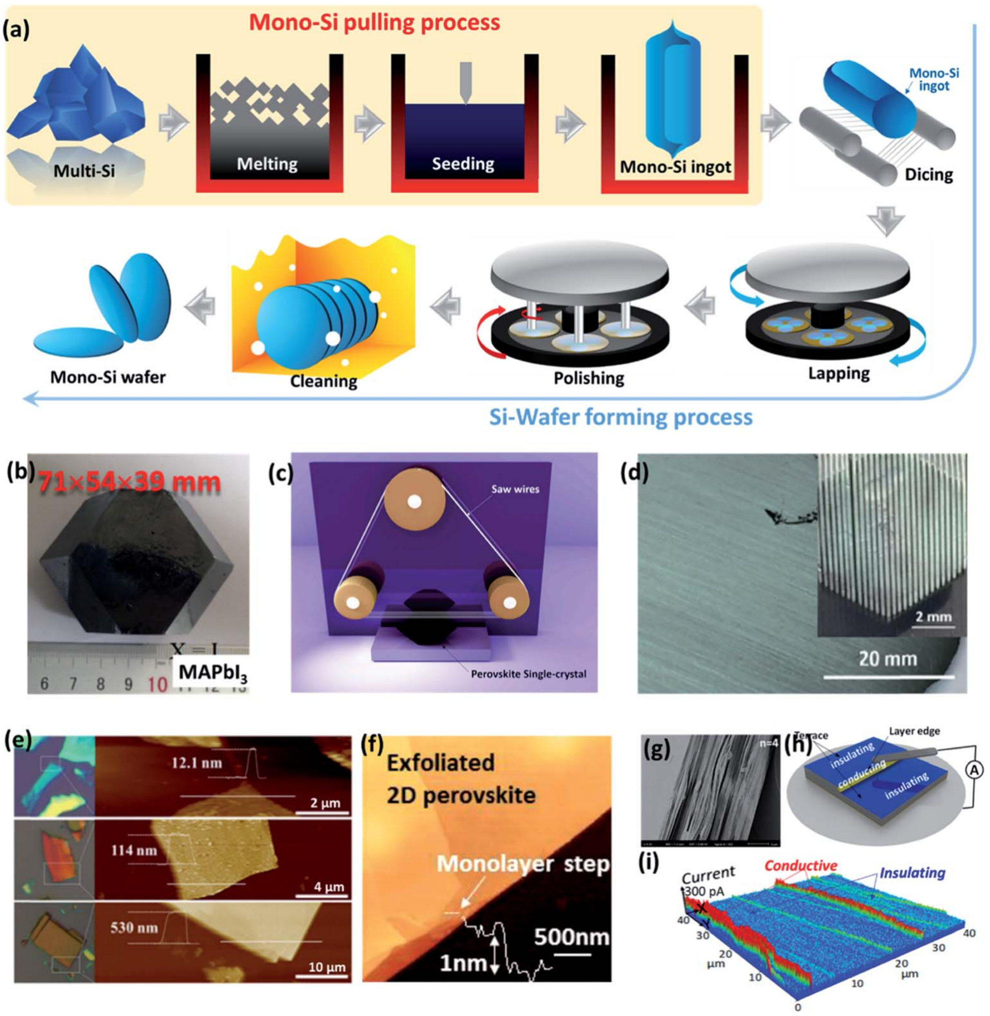


Fig. 7 Bulk-crystal dicing technology. (a) Industrial mono-Si wafer-manufacturing scheme showing the mono-Si ingot pulling process from multicrystalline silicon (multi-Si), through melting, seeding, and pulling. A Si wafer is formed from bulk mono-Si ingot dicing, lapping, polishing, and cleaning. Dicing technology for mono-HP wafer processing starting from (b) single HP bulk,[98] Copyright © 1999–2019 John Wiley & Sons, Inc., through (c) dicing by a diamond wire saw.[6] Copyright © 2018 Elsevier Inc. (d) An actual photograph showing a sliced mono-HP wafer of MAPbI$_3$.[85] Copyright © 2017, Science China Press and Springer-Verlag GmbH Germany. (e) Optical and AFM images of the exfoliated $(C_4H_9NH_3)_2(CH_3NH_3)_{n-1}Pb_nI_{3n+1}$ ($n = 3$) 2D perovskite microplates for different thicknesses.[96] © 2018 IOP Publishing Ltd. (f) AFM image with the height profile of an exfoliated layer. The layered structure of a Br-based perovskite with $n = 1$ is evident with a monolayer step of 1 nm, as shown in the inset.[97] Copyright © 2017 American Chemical Society. (g) Side-view SEM of a $(C_4H_9NH_3)_2(CH_3NH_3)_{n-1}Pb_nI_{3n+1}$ ($n = 4$) 2D mono-HP crystal.[54] Copyright © 2018 American Chemical Society. (h) A C-AFM setup detecting the layered edge of a 2D mono-HP crystal and (i) an example of C-AFM current mapping showing the conductive layered edge.[43] © 2019 American Association for the Advancement of Science.

the mono-Si ingot with minimum defects can be obtained. Wafer manufacturing starts by slicing into a raw wafer with the specified dimensions, followed by lapping, polishing, and cleaning processes (Fig. 7a). In accordance with the SEMI® standard, the ultraflat disk needs to be ultraclean, virtually free of microparticles or other impurities, and polished to have a mirror-like surface. With regard to Si PVs, the material needs to have high purity of 99.9999% (wt%); for chip applications, this value is 99.999999999%.[84]

For manufacturing mono-HP wafers, attempts relying on the bulk-crystal slicing technology have been reported since 2016. A large perovskite crystal (Fig. 7b) was sliced into thin wafers (Fig. 7d) at Xi'an LONGI Silicon Materials by Liu's group.[85] When compared with other slicing methodologies, such as laser cutting, inner circle slicing, multiple wire slicing, *etc.*, which usually crack or burn the crystal into fragments, a diamond wire sawing machine exhibited good compatibility to fabricate a complete mono-HP wafer. They optimized the conditions by using a diamond wire with a dimeter of 0.08 mm, and MAI-saturated IPA solution as the coolant, at a sawing speed of 20 m s^{-1} and feeding rate of 0.7 mm min^{-1}, yielding thin mono-HP wafers with a lateral size of 120 mm and thickness of ~100 μm.[85] It should be noted that perovskite materials have a lower Young's modulus (~19 GPa)[86] than that of Si (140–180 GPa)[87] and are extremely sensitive to moisture. These require particular protection when used for slicing perovskite materials. In particular, typical wire cutting and mechanical polishing could shrink the thickness of mono-HP wafers to ∼200 μm. However, further polishing upon this thickness level could easily cause mechanical damage due to its high fragility. Lv *et al.*[88] developed a wet-etching method to engineer the wafer thickness. They used the residual mother liquor that was used to grow the crystal to etch the surface of a mono-HP wafer. By immersing ∼200 μm-thick $MAPbI_3$ wafers in the etching solution by modulating the immersion time, temperature, and concentration, a desired thickness down to 15 μm could be achieved.[88] Similar wet-etching strategies can also be seen in the field of mono-Si wafer fabrication. For example, Lin *et al.*[89] reported the fabrication of a 30 μm-thick mono-Si chip using a chemical-etching method. Li *et al.*[90] obtained 18 μm-thick free-standing mono-Si membranes by the wet-etching of a 500 μm-thick wafer. Taking the advantage of mature slicing techniques used in the mono-Si field, such as its ability in controlling the crystal-facet orientation, flexibility in product dimension, technical maturity with streamlined and high throughput processes, and good compatibility with existing manufacturing market, transferring this technology to mono-HP wafer fabrication can be a promising direction. Nevertheless, several fundamental problems need to be taken into consideration before this transition, namely, (i) slicing- and lapping-caused surface defects; (ii) shortage of proper materials for surface treatment, such as damage etching, atomic-scale polishing, and ultrapure cleaning; (iii) concerns regarding the high sensitivity toward oxygen and moisture of perovskites; (iv) dynamic material degradation, cracking, brittle fracture, and poor mechanical properties; and (v) kerf loss.

On the other hand, following the nature of slicing a crystal in the mechanical aspect, another derivative is mechanical exfoliation, which has been widely employed in the field of traditional 2D materials, such as graphene and molybdenum disulfide (MoS_2). Lower-dimensional perovskites, such as the well-known $BA_2MA_{n-1}Pb_nI_{3n+1}$ (ref. 54) and $PEA_2MA_{n-1}Pb_nI_{3n+1}$,[91] have good compatibility with this technique because of their unique VDW heterostructures.[92,93] The inorganic $[PbI_6]^{4-}$ octahedral layer can be separated by the organic bilayers of BA or PEA, and the intermolecular interaction between the neighboring organic layers is the VDW bond, the bonding energy of which is several orders of magnitude lower than those of covalent and ionic bonds. This facilitates the exfoliation of several single-crystal layers from the bulk crystal. Peng *et al.*[94] prepared a 2D mono-HP wafer of $(C_6H_5C_2H_4NH_3)_2PbI_4\cdot(CH_3NH_3PbI_3)_{n-1}$ ($n = 1$, 2, and 3) using this method. Similarly, Niu *et al.*[95] reported mono- and few-layer-thick 2D mono-HP wafers of $(C_6H_9C_2H_4NH_3)_2PbI_4$. In particular, they found a clear difference in the exciton properties between the "bulk" (>15 layers) and very thin (<8 layers) regions, and they ascribed this to the structural rearrangement of the organic molecules around the inorganic sheets. Since mechanical exfoliation typically cannot yield a large complete sample with uniform layers, a hierarchical terrace-like feature with a planar inner terrace region and layered edge region is usually observed (Fig. 7e).[96] From Fig. 7f, it is evident that the exfoliated 2D perovskite exhibits a layered edge step,[97] quantified by the unit thickness multiplied by the number of layers. A side-view example of a $(C_4H_9NH_3)_2(CH_3NH_3)_{n-1}Pb_nI_{3n+1}$ ($n = 4$) 2D mono-HP crystal is shown in Fig. 7g.[54] These layered edges have been observed to have a conductive feature by means of conductive atomic force microscopy (C-AFM) measurements (Fig. 7h).[43] A topographical "insulating/conductive/insulating" feature across the layered edge (Fig. 7i) suggests potential applications in microscopic electronics.[43] Overall, in spite of these exciting findings involving 2D mono-HP thin films prepared from the mechanical exfoliation method, the inherent drawbacks such as low reproducibility, small area, and low homogeneity limit its scale-up applications.

4. Mono-HP PVs

The absence of GB and the significantly minimized trap densities in single crystals leads to the superb charge transport property and a scenario of approaching and even breaking the Shockley–Queisser limit. For example, recent investigations have revealed the below-bandgap absorption in mono-HP PVs, which could be expected to break the limit by taking advantage of photons in the NIR to IR region *via* an indirect band transition.[68] The findings of intrinsic twin domains in tetragonal $CH_3NH_3PbI_3$ HPs by Rothmann *et al.*[99] also provided additional room for relaxing the stress and strain within the perovskite lattice to improve the device performance. The persistent ferroelectric domains in $MAPbI_3$ mono-HPs, as confirmed by Garten *et al.*,[100] provided the necessary evidence for making early conjectures on the contribution from ferroelectric domain walls,[41,42,100] which can provide charge transport highways for photocarriers as well as the opportunity for "ferroelectric PVs" to surpass the Shockley–Queisser limit with the contributions from the ferroelectric domain wall.[101,102] Multiphoton excitations,[103,104] nonlinear optical properties,[105] and upconversion[106] phenomena observed in mono-HPs suggest their potential in taking the advantage of photons with longer wavelengths beyond the absorption edge. Recent discoveries involving photon recycling are analogous to a solar concentration effect,[45] and hot-carrier cooling to use the hot carriers before thermalization[44] in HPs can yield a potential PCE value of 66%. With regard to mono-HP PVs, designing and constructing device architecture that can maximize these effects is imperative to obtain proof-of-concept ultrahigh-performance devices.

4.1 Lateral mono-HP PVs

A solar cell can be constructed in either lateral or vertical architectures depending on the alignment between the photocarrier transport direction and illumination direction. Fig. 8 shows two examples of device architectures: lateral and vertical devices. Normally, in any solar cell, an internal electrical potential gradient (*e.g.*, "p–n junction" in a Si solar cell;[107] "electron donor–acceptor heterojunction" in an organic solar cell[108]) is required to form a depletion region that can be used to separate the photogenerated charge carriers and/or driving each type of carriers to their corresponding electrodes. This internal

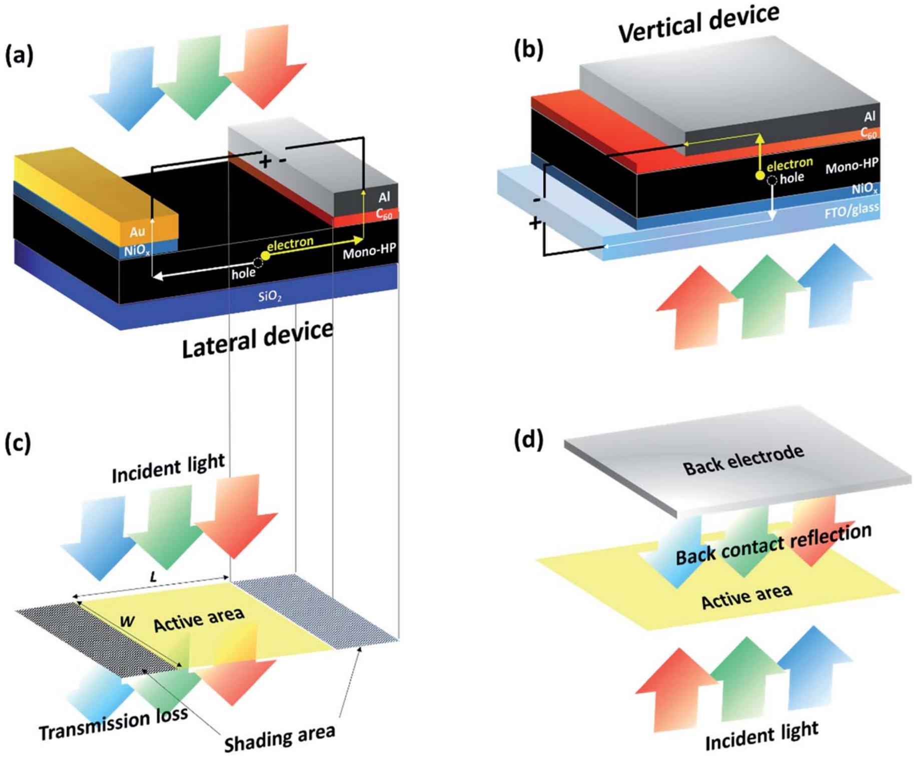


Fig. 8 Two examples of device architectures for mono-HP solar cells. (a) A lateral device structure where the photocarrier transport direction in the mono-HP is perpendicular to the direction of incident photons. (b) A vertical device structure where the photocarrier transport direction in the mono-HP is parallel to the direction of incident photons. Photoactive areas of the (c) lateral device and (d) vertical device.

electrical field can be provided by the work function difference of the electrode materials, heterostructures-induced potential gradient, dipole, space charge, and interfacial effects by various buffer layer materials.[109] Meanwhile, to passivate the surface traps, minimizing the Schottky barrier at the interface, with the help of various n-type and p-type interfacial modification materials, has been widely attempted in solar cells, photodetectors, and LEDs. Similarly, for mono-HP PVs, n-type buffer layers such as TiO_x,[108,110] ZnO,[111] SnO_2,[112] C_{60},[111] PCBM,[111,113] *etc.*, and p-type buffer layers such as PEDOT:PSS,[114] NiO_x,[115] Spiro-OMeTAD,[116] P3HT,[117] *etc.*, can also be used. Fig. 8a shows an example of a lateral device, where a mono-HP is supported by a SiO_2 substrate, and different electrodes (coupled with/without buffer layers) are separately deposited on the crystal, leaving an open channel area for receiving the photons. Such a design enables the fabrication of an entire device only on one side of the crystal; hence, the issues involving crystal thickness or the deposition of a transparent electrode can be ignored. However, one major drawback is the low usage of the light exposure area. As shown in Fig. 8c, there is a shading area of the electrode that can block light absorption, leaving a smaller uncovered open channel such that the effective device area becomes $L \times W$. In addition, such an area is limited by the charge-carrier diffusion length of mono-HPs. For example, when the channel length L exceeds the diffusion length (hyper-microscale), the photogenerated charge carriers are prone to recombination to result in energy loss before arriving at the electrodes. Meanwhile, the deficiency of back-contact reflection also leads to a large optical transmission loss (Fig. 8c). A combination of these factors leads to low PCEs for lateral mono-HP PVs. An early attempt for lateral mono-HP PVs relies on a piezoelectric poling effect to induce device asymmetry.[118] Dong *et al.*[118] reported a strong piezoelectric effect in $MAPbI_3$ mono-HPs (Fig. 9a), which enables poling within single crystals under a nonuniform electric field. The strain-generated GBs provide paths for ion migration and finally form a *p–i–n* structure (Fig. 9b). As a result, a lateral Au/mono-HP/Au device with sufficient poling treatment exhibits a V_{OC} value of 0.61 V, J_{SC} value of 2.28 mA cm^{-2}, and PCE value of 1.88% (Fig. 9c). In spite of its low PCE value, the lateral mono-HP PV device can form a new route toward fabricating efficient low-cost solar cells due to its simple device configuration of metal/mono-HP/metal. Such a design eliminates the need for more expensive transparent electrodes. Meanwhile, instead of electrical poling, intentionally doping the mono-HP and/or introducing n-type and p-type buffer layers at the cathode and anode, respectively, to preserve longer carrier depletion length is a good way to improve the PCE. By modifying the buffer layer interface, Lee *et al.*[77] designed a mono-HP solar cell using metal electrodes with different work functions and a n-type cathode buffer layer of PCBM (Fig. 9e and f). The best lateral mono-HP device exhibits a J_{SC} value of 18.33 mA cm^{-2}, V_{OC} value of 0.801 V, fill factor (FF) value of 0.329, and PCE value of 4.83%, which is significantly higher than the polycrystalline lateral device with a maximum PCE value of 0.194% (Fig. 9f). This can

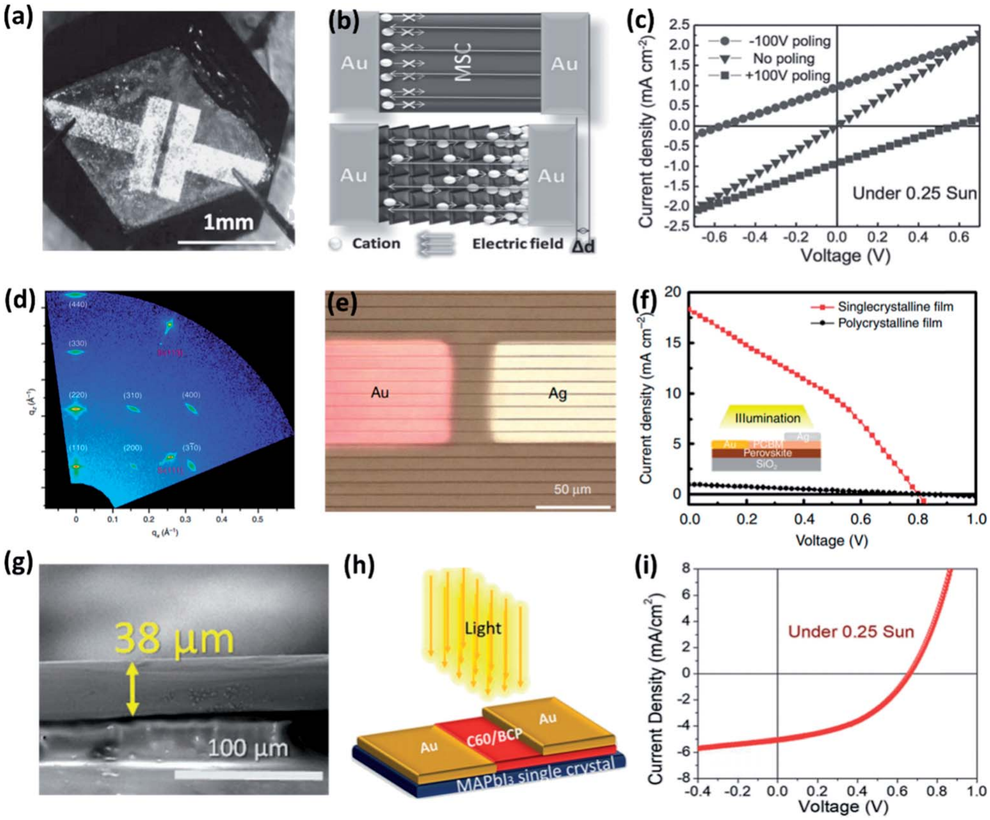


Fig. 9 Lateral mono-HP device and performance. Piezoelectric poling strategy for antisymmetric devices. (a) Image of $MAPbI_3$ lateral structure single-crystal device. (b) Scheme of electromechanical-strain-generated GBs and ion migration in mono-HPs. (c) Switchable PV effect of a $MAPbI_3$ lateral mono-HP solar cell with positive and negative poling.[118] Copyright © 1999–2019 John Wiley & Sons, Inc. Buffer layer strategy for antisymmetric devices. (d) Two-dimensional X-ray diffraction (2D XRD) image of a mono-HP thin film. (e) Optical microscopic image of a lateral mono-HP solar cell with metal electrodes. The light brown and dark brown lines indicate mono-HPs and spaces, respectively. (f) *J*–*V* curves of single-crystalline (red) and polycrystalline (black) perovskite thin films with lateral mono-HP cells. The inset shows a schematic device structure of a lateral perovskite solar cell and the direction of illumination.[77] Copyright © 2017, Springer Nature. (g) SEM images of the cross-section of a $MAPbI_3$ mono-HP wafer. (h) Scheme of $MAPbI_3$ mono-HP lateral-structure solar cell. (i) *J*–*V* curve showing a PCE value of 5.9%.[57] Copyright © 1999–2019 John Wiley & Sons, Inc.

be ascribed to the higher mobility, *i.e.*, 45.64 $cm^2\ V^{-1}\ s^{-1}$, of mono-HPs as compared to that of polycrystalline films (0.2512 $cm^2\ V^{-1}\ s^{-1}$). Similarly, Liu *et al.*[57] constructed an analogous device structure using C_{60}/BCP as the cathode buffer layer (Fig. 9g–i). The lateral device exhibits a PCE value of 5.9% under sunlight of 0.25, yielding a J_{SC} value of 5.06 mA cm^{-2}, V_{OC} value of 0.66 V, and FF value of 0.44. As the single crystal has an extremely low trap density within its crystal, SRH recombination losses may still occur at the crystal surface. Technically, the surface trap is the major reason for such low efficiencies in terms of recombination losses. Modifications on the mono-HP surface to minimize the trap density using learnings from various interfacial modification cases is expected to improve the device efficiency.

With diffusion lengths of several micrometers (*e.g.*, 175 μm in the prototype $MAPbI_3$ single crystal), a thinner wafer is imperative in terms of depletion width and diffusion length, either of which can set up the limit distance for charge traveling before recombinations. Otherwise, a thicker film can cause charge loss in the region beyond the limit distance. However, handling an ultrathin wafer with micrometer-scale thickness seems to be practically challenging. Alternatively, enhancing the diffusion length/depletion width by proper doping may provide solutions to this thickness issue. Since the ultimate goal is to secure sufficient charge carriers reaching the electrodes and thereby minimizing charge loss from recombinations, an introduction of a localized electrical field, particularly at the interface, can sufficiently adjust the depletion region and regulate the drift–diffusion balance, which can sufficiently improve the device performance. For example, the employment of an ionic liquid in light-emitting electrochemical (LEC) cells,[119,120] can provide mobile ions that are driven to the boundaries under bias at elevated temperatures and frozen at room temperature to yield an ion-generated electrical field. This electrical field can help charge separation and transport in the device. A similar mechanism facilitating the charge separation, extraction, transport, and collection can be found in OPVs, where such a localized electric field can be provided by the interfacial "dipoles",[121] coercive electrical field from functional nanoparticles,[122] and functional ferroelectric interlayers.[123] In the case of perovskites, constructing a *p–i–n* structure by perovskite self-doping is a worthwhile attempt to break the electrode symmetry and simplify the device architecture by eliminating the necessity for expensive transparent conductive electrodes (TCEs). Typical methods that include electrical poling induced by ion migration and self-doping dominantly rely on the GB that provide the ion migration path in polycrystalline perovskites.[124] However, in single-crystal perovskites, since the energy barrier for ion migration within the single-crystal domain is twice that at the GB, ion-assisted self-doping seems to be difficult to realize in single-crystal perovskites. However, a primitive demonstration on the self-doping of a single-crystal perovskite through the "piezoelectric poling" effect[118] can be a good attempt.

Alternatively, since the "space-limited growth method" enables direct perovskite crystal growth on a transparent conductive substrate, building the device upon these single-crystal membranes coated with transparent electrodes can be considered to be promising. Therefore, various strategies growing mono-HPs on FTOs and/or ITO substrates and constructing the solar cell device upon it have been reported, which turns out into a "vertical device".

4.2 Vertical Mono-HP PVs

To better accommodate the crystal dimensions with the carrier diffusion length, a vertical mono-HP device design incorporating mono-HPs with microscale thickness or smaller has been proposed, which can eventually yield higher efficiency. The earliest mono-HP vertical device was built based on a bulk single crystal of $MAPbI_3$ with millimeter thickness[49] (such a device is shown in Fig. 10a). Bearing the maximal diffusion length of 175 μm for $MAPbI_3$ single crystals, such a large thickness causes dramatic charge carrier recombinations during vertical transport through the bulk single crystal.[98,125] Furthermore, to induce electrical asymmetry for separate electron and hole collections, different metals, such as Ga and Au, were used as the electrodes. This design is not compatible for solar cell applications as no light path can pass through any electrode; rather, it is good for gamma-voltaic applications.[49] Using an intense cesium-137 source, a gamma-voltaic PCE value of 1.73% can be achieved. Constructing solar cell devices based on mono-HPs requires a small crystal thickness. A study focusing on the PCE dependence on mono-HP thickness in mono-HPs of $MAPbBr_3$ was reported by Peng *et al.*[126] As shown in Fig. 10b, they tuned the mono-HP thickness from 4 to 60 μm, and modified the cathode side with an n-type buffer layer, namely, TiO_2. The device with mono-HPs of smaller thicknesses delivered higher PCE due to the significantly improved FF. This is because FF is closely correlated with the charge carrier mobilities in the device. A larger FF in a thinner mono-HP device yields improved carrier mobilities. Using a simple ITO/mono-HP/Au structure without any buffer layers, a nearly 100% internal quantum efficiency (IQE) and PCE > 5% can be obtained.[126] In fact, modifying the electrode further improves the PCE value to 6.5% with a remarkable V_{OC} value of ~1.4 V.[126] The positive role of interface engineering has been evidenced in the mono-HP device. It should be noted that the $MAPbBr_3$ mono-HPs have a cubic crystal structure at room temperature and they are easier to grow than $MAPbI_3$ mono-HPs. Hence, several early attempts involving mono-HP devices were made for fabricating on the $MAPbBr_3$ material. Rao *et al.*[66] also utilized $MAPbBr_3$ mono-HPs to construct solar cells (Fig. 10c). In particular, they modified both cathode and anode with different buffer layers, *i.e.*, TiO_2 and spiro-MeOTAD, respectively, to minimize the Schottky barrier. A $MAPbBr_3$ mono-HP with a thickness of 16 μm and a size of 6 × 8 mm^2 exhibits the highest PCE value of 7.11%. Another milestone for mono-HP devices can be seen in $(FAPbI_3)_{0.85}(MAPbBr_3)_{0.15}$ mono-HPs.[127] Such a mixed mono-HP is believed to deliver high photocurrents due to the smaller bandgap of $FAPbI_3$. With NiO_x and TiO_x interfacial modification layers (Fig. 10d), the device has better extraction and anticharge blocking effect, yielding a PCE value of 12.18%. Later, in 2017, Chen *et al.*[68] fabricated the $MAPbI_3$ mono-HP solar cell with a decent PCE value of 17.8%. By adjusting the thickness at the level of tens of micrometers, they found that the spectral response of $MAPbI_3$ mono-HP solar cells could be extended to 820 nm, which is 20 nm broader than the corresponding polycrystalline thin-film solar cells. They ascribed these phenomena to the indirect bandgap absorption or Urbach band tail, which may challenge the Shockley–Queisser limit by the utilization of additional photons. The highest PCE value of mono-HP devices was reported in 2019, with an efficiency of 21.09% (ref. 128) for $MAPbI_3$ mono-HP devices. By decreasing the thickness to ~20 μm and employing a device structure of ITO/poly(triarylamine) (PTAA)/$MAPbI_3$ mono-HP/C_{60}/BCP/Cu, a J_{SC} value of 23.46 mA cm^{-2}, V_{OC} value of 1.076 V, and FF value of 83.5% could be achieved. It should be noted that such values are measured in an inert nitrogen atmosphere. They observed that the performance could drastically deteriorate when the measurements were performed under ambient conditions (22 °C, 50–55 RH), particularly with respect to the J_{SC} value.[128] Overall, the mono-HP device seems to be more promising in achieving ultrahigh device performance as compared to their polycrystalline counterparts. However, current studies have revealed a generally lower PCE value of mono-HP solar cells as compared to poly-HP devices. The major reason is the thickness of the mono-HP layer, which is extremely difficult to control at the sub-micrometer scale, notwithstanding the surface homogeneity and surface traps of the mono-HPs.

Clearly, beyond this concern regarding thickness, buffer layers that can induce a depletion region, extract charge carriers, and select/block and transport/collect electrons or holes, are also crucial to the overall PCE. The functionality of these buffer or interfacial modification layers is similar to those already applied in photoelectronics when using polycrystalline perovskite thin films.[108] Besides traditional small-area devices, incorporating a perovskite single crystal into a large-area solar module has also been researched. A good attempt can be seen in the wafer-scale mono-HP patterned thin films based on geometrically confined lateral crystal growth, which involves a 3 × 3 in^2 solar module with a PCE value of 4.83%.[77] It should be mentioned that the (i) lateral device structure with long lateral

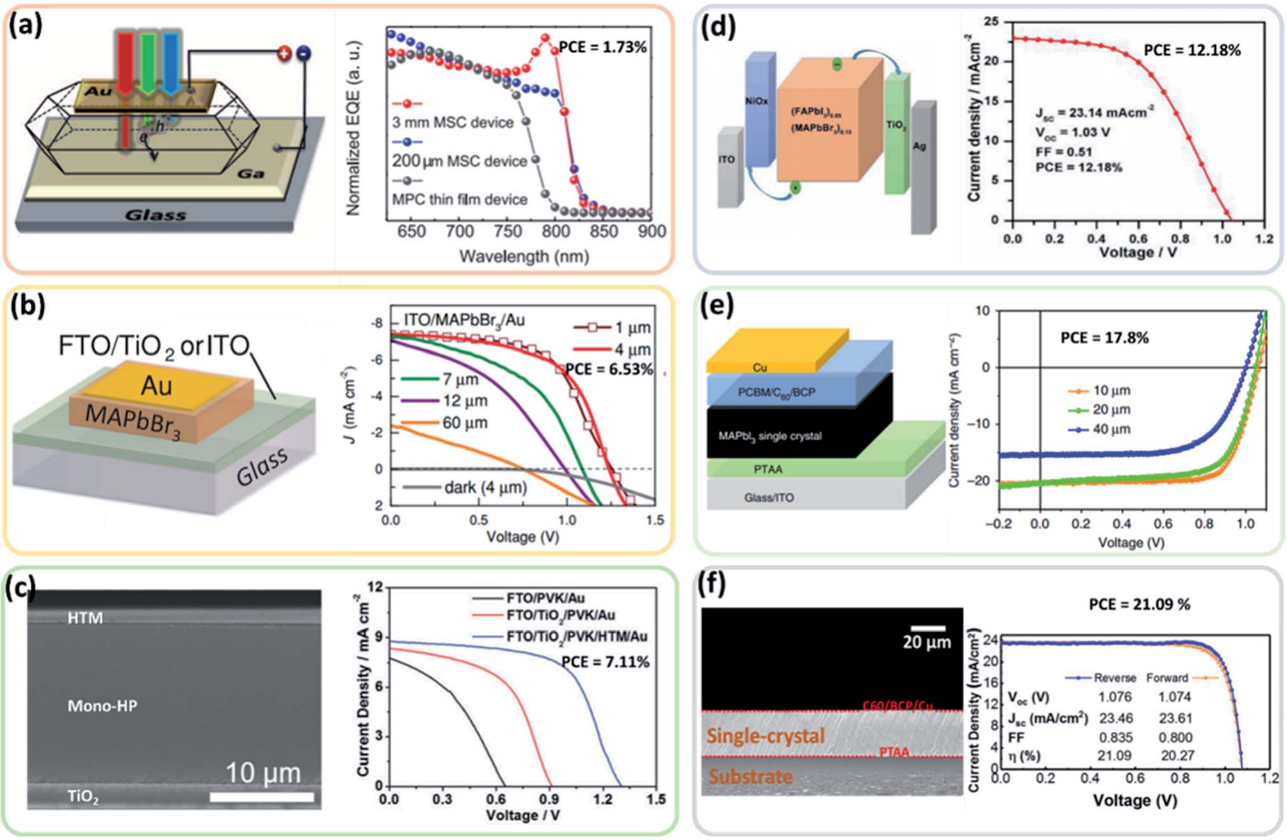


Fig. 10 Milestone vertical mono-HP device and performance. (a) Schematic device structure of the $MAPbI_3$ mono-HP devices. Normalized EQE values of 3 mm-thick and 200 mm-thick $MAPbI_3$ mono-HP devices as compared to that of a thin-film device.[49] Copyright © 2015, American Association for the Advancement of Science. (b) $MAPbBr_3$ mono-HP devices with/without a cathode buffer layer and device performance of the device based on $MAPbBr_3$ mono-HPs of different thicknesses.[126] Copyright © 1999–2019 John Wiley & Sons, Inc. (c) Cross-sectional SEM image of $MAPbBr_3$ mono-HP devices with the highest PCE value of 7.11%.[67] © The Royal Society of Chemistry 2017. (d) Band alignment and *J*–*V* curve of the highest PCE value of mono-HP devices using ITO/NiO_x/$(FAPbI_3)_{0.85}(MAPbBr_3)_{0.15}$/$TiO_2$/Ag.[127] Copyright © 1999–2019 John Wiley & Sons, Inc. (e) Device structure and *J*–*V* curve of single-crystal devices using $MAPbI_3$ mono-HPs with different thicknesses. A PCE value of 17.8% has been obtained.[68] Copyright © 2017, Springer Nature. (f) Cross-sectional SEM image of a $MAPbI_3$ mono-HP device with *J*–*V* curves showing a record PCE value of 21.09%.[128] Copyright © 2019 American Chemical Society.

distance between electrodes and (ii) improper contact with a direct electrode without a buffer layer may act as the main reasons for the insufficient PCE. In addition, other device structures fabricated by different manufacturing methods, such as "top-down approaches",[129] atomic scissoring,[130] molecular bonding, self-assembled monolayer (*e.g.*, APTES)-assisted bonding,[47] and "sandwiching of two slides",[131] may bring additional insights into the processing requirements. Overall, however, only sophisticated techniques capable of growing homogeneous, flat, surface-trap-free, thin, and large mono-HP wafers/thin films have been developed because of which the efficiencies could further compete with those of poly-HP devices.

4.3 Ultrahigh PCE

Although, in principle, single-crystal devices could outperform their polycrystalline counterparts because of the absence of GB and minimal defect density, the current device performance is still unsatisfactory. Table 1 summarizes the performance parameters of the state-of-the-art single-crystal perovskite solar cells proposed in last three years. The PCE values are in the range from 0.75% to 21.09%, where most of the works reported PCE < 10%, which is clearly lower than the typical value of their polycrystalline counterparts (*ca.* 18% from various current studies). The inferiority in PCE can be associated with several factors: (i) surface trap. Although the bulk trap density is several orders of magnitudes lower in single crystals, it should be noted that a large density of surface traps still exist,[132] which can induce ionic charges due to the uncoordinated sites on the surface. To finely tune the surface properties, methods such as surface passivation by fullerene,[133] ionomer,[134] ionic liquid,[120] and Lewis base,[135] as well as compositional regulation by argon plasma treatment (APT),[136] have been applied. In addition, the structural asymmetry at the surface can induce nontrivial physical properties, particularly in lower-dimensional perovskite materials. Recently, we found highly conductive crystal edges in 2D BA_2PbI_4 perovskite MQW structures exhibiting a super high carrier density of 10^{20} cm^{-3}, approaching those observed in metals. As several intrinsic surface properties of

Table 1 Performance parameters of state-of-the-art mono-HP devices

Device type	Device architecture	Light source	Thickness	J_{SC} (mA cm^{-2})	V_{OC} (V)	FF	PCE (%)	Ref.
Vertical	ITO/PEDOT:PSS/$MAPbI_3$/PCBM/Ag paste or Al			0.04	0.55	34.1	0.75	129
Vertical	ITO/PEDOT:PSS/$MAPbI_3$/PCBM/ZnO/Al	AM 1.5 G	300 nm–3 mm	8.69	0.52	0.38	1.73	139
Vertical	Ga/$MAPbI_3$/Au	Intense cesium-137 source	3 mm				3.90	49
Vertical	ITO/PEDOT:PSS/$MAPbI_3$/PCBM/Ag	AM 1.5 G	50 μm	22.15	0.75	0.27	4.40	140
Vertical	ITO/$MAPbBr_3$/Au	AM 1.5 G	1 μm	7.39	1.25	0.59	5.49	126
Vertical	ITO/$MAPbBr_3$/Au	AM 1.5 G	4 μm	7.42	1.24	0.58	5.37	
Vertical	ITO/$MAPbBr_3$/Au	AM 1.5 G	7 μm	7.19	1.11	0.46	3.7	
Vertical	ITO/$MAPbBr_3$/Au	AM 1.5 G	12 μm	7.09	1.03	0.39	2.82	
Vertical	ITO/$MAPbBr_3$/Au	AM 1.5 G	60 μm	2.27	0.94	0.31	0.65	
Vertical	FTO/TiO_2/$MAPbBr_3$/Au	AM 1.5 G	1 μm	6.69	1.36	0.69	6.53	
Vertical	FTO/$MAPbBr_3$/Au	AM 1.5 G	16 μm	7.77	0.65	0.39	1.98	67
Vertical	FTO/TiO_2/$MAPbBr_3$/Au	AM 1.5 G	16 μm	8.35	0.91	0.53	4.08	
Vertical	FTO/TiO_2/$MAPbBr_3$/HTM/Au	AM 1.5 G	16 μm	8.77	1.31	0.62	7.11	
Vertical	FTO/TiO_2/$MAPbI_3$/Spiro-OMeTAD/Ag	AM 1.5 G		22.283	0.668	0.59	8.78	141
Vertical	ITO/NiO_x/$(FAPbI_3)_{0.85}(MAPbBr_3)_{0.15}$/$TiO_x$/Ag	AM 1.5 G	24.5 μm	23.14	1.03	0.51	12.18	127
Vertical	ITO/PTAA/$MAPbI_3$/PCBM/C_{60}/bathocuproine (BCP)/Cu	AM 1.5 G	10 μm	21	1.08	0.786	17.80	68
Vertical	ITO/PTAA/$MAPbI_3$/$PC_{61}BM$/C_{60}/BCP/Cu	AM 1.5 G	15 μm	21.2	1.05	0.73	16.30	136
Vertical	ITO/PTAA/$MAPbI_3$/$PC_{61}BM$/C_{60}/BCP/Cu, w/APT treatment for 2 s	AM 1.5 G	15 μm	22.5	1.11	0.816	20.40	
Vertical	ITO/PTAA/$MAPbI_3$/C_{60}/BCP/Cu	AM 1.5 G	~20 μm	23.46	1.076	0.835	21.09	128
Lateral	Au/$MAPbI_3$/PCBM/Au	AM 1.5 G		3.84	0.802		4.83[a], 6.6[b]	77
Lateral	Au/$MAPbI_3$/Au, piezoelectric poling treatment	25 mW cm^{-2} (0.25 sun)		2.28	0.82		5.36[c], 1.88[d]	118
Lateral	Au/$MAPbI_3$/C_{60}/BCP/Au	25 mW cm^{-2} (0.25 sun)		5.06	0.66	0.44	5.9	57

[a] Average PCE. [b] Champion PCE. [c] Obtained at 170 K. [d] Obtained at room temperature.

perovskite crystals still remain unclear, further physical and chemical investigations may bring new insights. (ii) Surface hydration. Structural asymmetry can yield terminal crystallographic ions that are vulnerable to various environmental stimuli, such as moisture and oxygen.[137] Definitely, single-crystal devices with hydrated facets form poor contact with electrodes, resulting in higher leakage currents and severe resistive losses despite their excellent bulk properties. Overcoming the integration challenges associated with hydrated or degraded interfaces require a profound understanding of the surface characteristics and eventual chemical transformation.[138] (iii) Buffer layer. In any solar cell, the buffer layer is crucially important for efficient extraction and transport of certain types of charges to the electrodes. In this context, the energy level, mobility, transparency (front layer), and stability need to be basically considered. Various relevant studies involving OPVs, DSSCs, Si, and GIGC solar cells can be revisited taking into consideration buffer layer materials.[108] (iv) Thickness tradeoff. Thicker single-crystal wafers enable indirect band absorption (and therefore higher photocurrent) and can facilitate handling and processing, but they can also introduce more traps and increase recombination loss. Therefore, balancing the potential risk in recombination loss by designing a suitable thickness of mono-HP needs to be carefully considered.

4.4 Device stability

The public acceptance of HP PV technology is based on its reliability not only in terms of higher efficiency but also satisfactory lifetime. HP materials suffer from low stability against moisture, heat, and radiation.[142] The stability problem can be resolved by understanding mono-HP devices.

Moisture is usually regarded as the chief culprit for device degradation involving HP PVs. In the presence of moisture, various degradation mechanisms, such as the formation of hydrate products of $(MA)_4PbI_6\cdot 2H_2O$,[143] phase transition from α to δ in $FAPbI_3$ and $CsPbI_3$ systems,[144,145] *etc.*, have been researched. Moisture infiltration into the inner perovskite typically starts from the GBs[146] and a high trap density can facilitate moisture-induced degradation *via* an ion migration mechanism.[146,147] Because of the virtue of ultralow trap density and absence of GBs, mono-HPs are expected to have years of stability in air. For example, an unencapsulated $MAPbI_3$ mono-HP device can endure for 30 days in dark air (23 °C and 30% RH), showing no degradation.[68] A mono-HP device using the structure of FTO/TiO_x/mono-HP/spiro-MeOTAD/Au has been reported to maintain 93% of its initial PCE after aging for 1000 h.[66] The all-inorganic $CsPbBr_3$ mono-HP device exhibits 3 month stability in air with 20% RH at room temperature.[83] It should be noted that all these devices are freshly made and no further encapsulation techniques need to be applied. Recent wrapping methods, such as atomic-level protection using the fluorination treatment,[148] can also be used for these mono-HP devices for prolonging their lifetime.

In addition to moisture, heat can also induce stability issues, such as phase transitions and chemical decomposition. For example, $MAPbI_3$ can experience phase transition from the tetragonal ($I4cm$) to cubic ($Pm\bar{3}m$, $Z = 1$) phase when the temperature increases up to 327 K (~54 °C).[149] In poly-HPs, the decomposition at the GBs can be triggered at relatively lower temperatures and accelerated at elevated temperatures due to the corrosive contaminants that are typically stored in the voids and GBs. For example, the $MAPbI_3$ poly-HP thin film usually exhibits a decomposition temperature of ~150 °C, while mono-HP wafers can sustain themselves at far higher temperatures (up to 240 °C).[65] Similarly, mono-HP wafers of $MAPbCl_3$, $MAPbBr_3$, and $FAPbI_3$ have been reported to have higher decomposition temperatures of 214, 257, and 300 °C, respectively.[46] In addition, for the all-inorganic perovskite of $CsPbI_3$, this temperature can go up to 567 °C until melting, which not only exhibits good thermal stability but also provides a potential way for casting a crystal film using the "melting method".[150,151]

Photoinduced-degradation processes can prove to be another mechanism that can induce the degradation of HP devices, as the ions in mono-HPs can be activated upon photon radiation and the migration of these ions and photocatalytic effects can trigger damaged contacts at the interfaces between the different layers.[152–154] The GBs and trap states are known to accelerate ion migration by providing percolation pathways,[147,155–158] which together with photon energy that activates the ions, can lead to photodegradation processes in poly-HP devices. In contrast, the mono-HP can be a good platform to reduce and/or eliminate ion migration and hence mass-transport-induced material degradation. In particular, for (quasi-)2D perovskite materials that have extremely low in-plane and out-of-plane ion migration properties,[159] the degradation induced by mass transport (ion migration) can be circumvented.

5. Mono-HP transistors

HP materials display extremely low effective mass of electrons and holes and hence large carrier mobilities as well as ambipolar transport characteristics,[160–162] which makes them a good candidate for use in field-effect transistors (FETs). However, a limited number of research efforts have been conducted along this direction due to device unreliability. Ion migration and accumulation at the interface of the dielectric layer and gate-field screening effect in HP polycrystalline films[158,163] can substantially reduce the charge carrier mobility that damages the normal functionality of a transistor device. Minimizing ion migration in poly-HP materials *via* the application of mono-HPs can be a promising solution to mitigate or even overcome such gate-field screening effects.

5.1 Ion migration influence

The protype HP material, $MAPbI_3$, with experimentally determined large intrinsic charge carrier mobility and ambipolar conductivity seems to be a good material for transistor applications. However, several studies from different research teams have coincidently found that $MAPbI_3$-poly-HP-based devices only exhibit FET characteristics at very low temperatures, but no FET behavior can be observed at room temperature.[164–166] Building upon $MAPbI_3$ poly-HP thin films, Chin *et al.*[164] fabricated the first light-emitting FET in 2015 (Fig. 11a). Using a bottom contact/bottom gate (BC/BG) device configuration and spin-coated $MAPbI_3$ poly-HP film on prepatterned Au/Ni (50 nm/10 nm) electrodes, tunable electroluminescence was observed in a lower temperature range from 78 to 178 K *via* the mechanism of recombination of balanced electron and hole injection from the opposite metal electrodes. The linear regime in the drain-to-source voltage, $V_d = \pm 20$ V, was obtained at 78 K, while both electron and hole mobilities drop quickly upon temperature increase (Fig. 11a(iv)); no transistor characteristics were observed at room temperature. They attributed the absence of room-temperature transistor characteristics to the ion screening effects, which were associated with the presence of ions accumulated at the perovskite/dielectric interface that block further charge injection.[164] Similarly, Labram *et al.*[165] fabricated a top contact/bottom gate (TC/BG) FET using spin-coated $MAPbI_3$ poly-HP films with aluminum electrodes on top, as shown in the inset of Fig. 11b. They found that the electrical characteristics exhibited low source–drain currents and no field-induced current modulation at room temperature, but there was a field effect below 220 K and the drain current continued to increase as the temperature further decreased. This might be linked to the temperature dependence of charge carrier mobility (Fig. 11b(ii)). Further, a screen mechanism was provided, as the $MAPbI_3$ might exhibit substantial polarization susceptibility to an electric field through mobile ions or alignment of the dipolar molecular cation; further, these polarization responses would lead to an electronic screen layer that electrically block that field (see Fig. 11b(iii)). Such a mechanism is expected to result in a screening of the applied gate voltage in the FETs, thereby inhibiting carrier accumulation and electrical conductivity of the channel. Both polarization due to local molecular motion and diffusion of ionic species in the HP solid are expected to be temperature-activated.[167–169] Simultaneously, ion migration is closely related with the activation energy of the ions; further, in poly-HP films with high GB and trap densities, such active ions and vacancy can be considerably higher. This induces a higher ionic contribution to poorer-quality poly-HP films. Inversely, the optimization of poly-HP films to reduce the GB and trap density can be an avenue to fabricate efficient FET devices. For example, Senanayak *et al.*[163] reported that through the optimization of the microstructure of a poly-HP film, as well as making modifications at the source–drain contact, it is possible to significantly minimize the instability and hysteresis in FET characteristics and demonstrate an electron field-effect mobility value of 0.5 $cm^2\ V^{-1}\ s^{-1}$ at room temperature. Briefly, they employed a $Pb(Ac)_2$-based precursor mixture and acquired a uniform thin film with a small root-mean-square (RMS) roughness value of ~5.4 nm. By optimizing the device by tuning the grain size from 38 to 150 nm by adjusting the precursor concentrations, modifying the gold

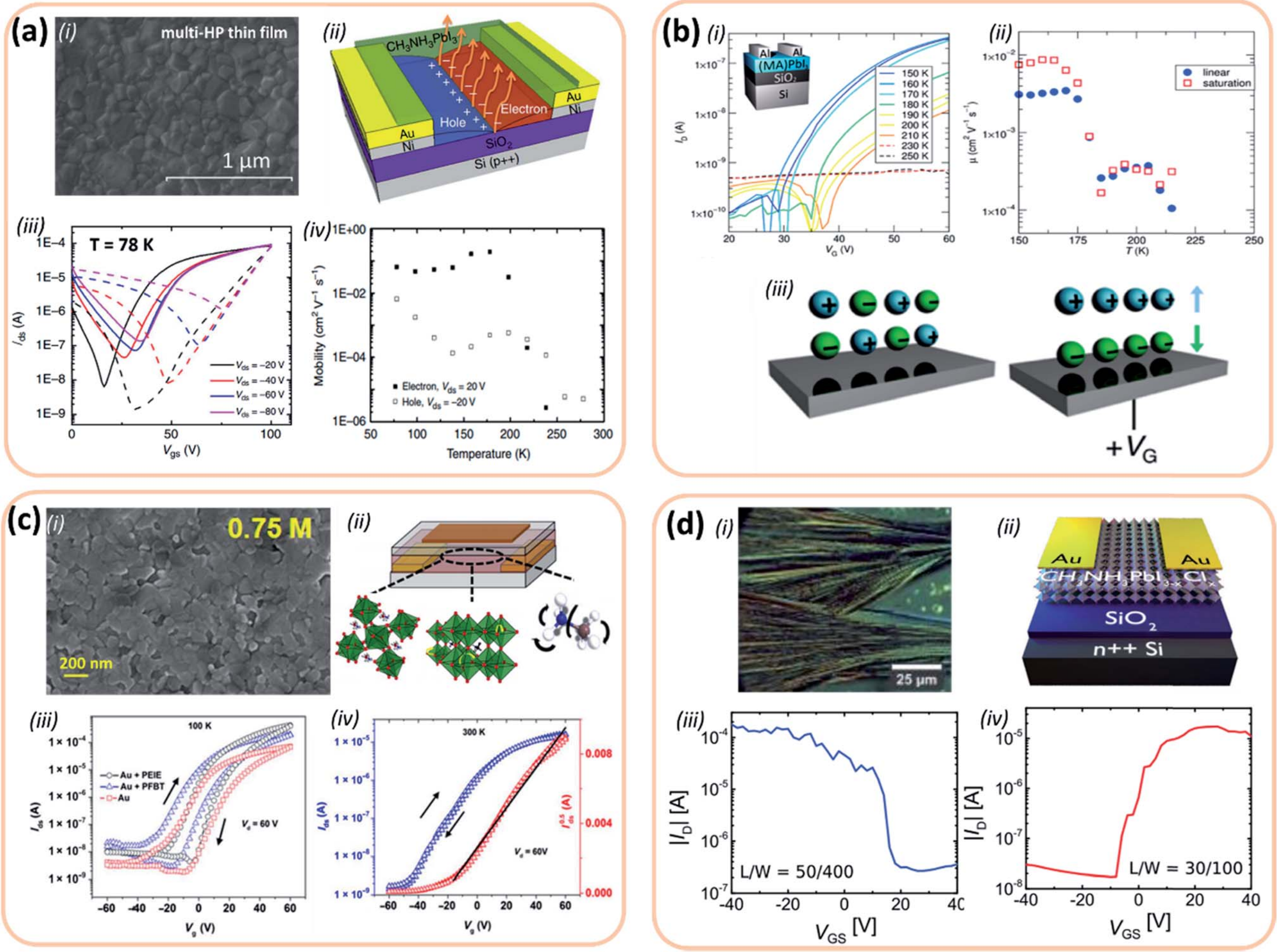
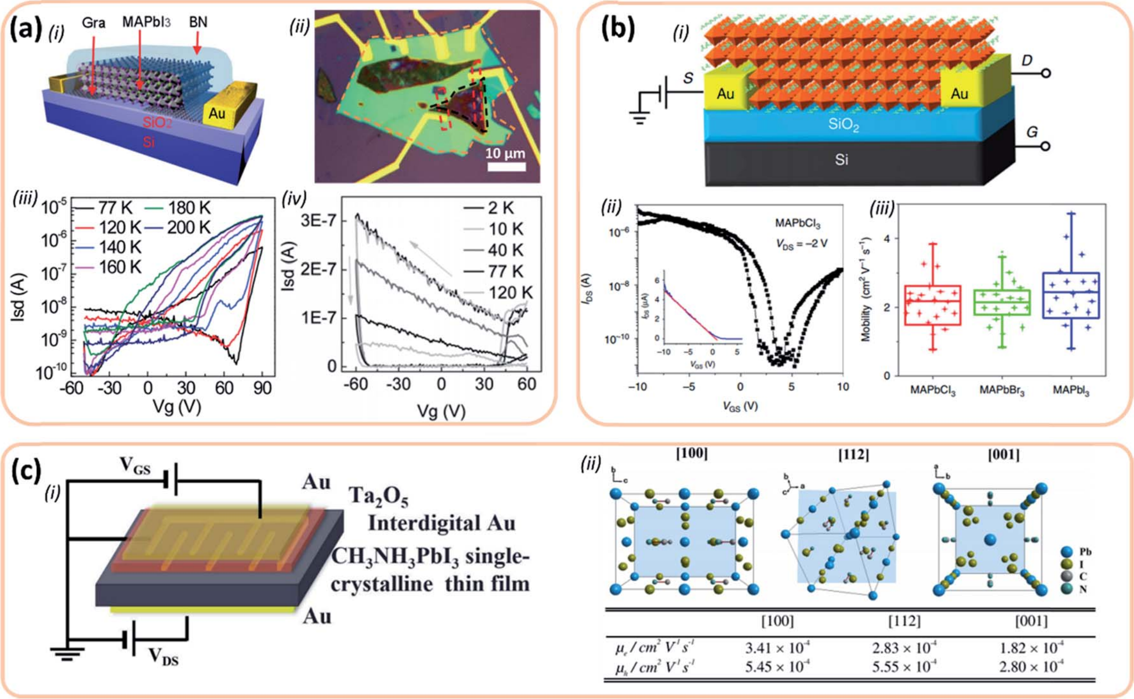


Fig. 11 Poly-HP FETs. (a) $MAPbI_3$ poly-HP film (i) and corresponding FET device configuration (ii). Transfer characteristics obtained at 78 K (iii). Temperature dependence of the field-effect electron and hole mobilities (iv).[164] Copyright © 2015, Springer Nature. (b) Transfer curves of $MAPbI_3$ poly-HP FETs measured at various temperatures between 150 and 250 K. The device has a length and width of 200 and 2600 μm, respectively, and the geometric capacitance of the dielectric was 23 nF cm^{-2}. Inset: schematic representation of the FET. Si labels the silicon gate electrode; SiO_2, 150 nm silicon oxide dielectric; $(MA)PbI_3$, the semiconductor layer; and Al, the aluminum source and drain electrodes (i). Approximate field-effect mobility evaluated using the gradual-channel approximation as a function of measurement temperature (ii). Schematic illustration of the proposed polarization mechanism of mobile ionic species in $MAPbI_3$ poly-HP under the influence of externally applied gate field (iii).[165] Copyright © 2015 American Chemical Society. (c) SEM images of an optimized $MAPbI_3$ mono-HP film fabricated from 0.75 M precursor solutions (i). Schematic of the top-gate bottom-contact poly-HP FETs summarizing the different sources of disorder mechanisms prevalent in a perovskite (left: vibrations of inorganic cage; middle: defect migration; right: MA^+ polarization disorder) (ii). Transfer characteristics at 100 K for different source–drain contact modifications (iii) and 300 K for PEIE-treated Au contacts (iv).[163] © 2017 American Association for the Advancement of Science. (d) Optical microscopic image of the $MAPbI_{3-x}Cl_x$ poly-HP film in the channel region after 20 min of solvent exposure; note the formation of large needle-shaped crystals (i). Poly-HP FET geometry (ii). Representative plot of I_D–V_{GS} characteristics ($V_{DS} = \pm40$ V) for holes (iii) and electrons (iv), respectively. The values of channel lengths and widths are shown in the inset.[170] Copyright © 1999–2019 John Wiley & Sons, Inc.

source–drain contacts with self-assembled monolayer (SAM) of pentafluorobenzenethiol (PFBT, ∼1 nm), and polymer surface modification layer of polyethylenimine ethoxylated (PEIE, ∼2 nm), excellent room-temperature n-type transfer behavior could be realized in a $MAPbI_3$ FET device, showing negligible hysteresis.[163] Similarly, Zeidell *et al.*[170] employed the solvent vapor annealing method to adjust the microscopic structure of poly-HP films. As shown in Fig. 11d(i), vapor annealing treatment can foster crystal formation with needle-like features. Further, by controlling the experimental conditions, a significant morphological change can be induced, where the preferential orientation can be modulated and grain size can be drastically increased with healing of GBs into intermediate phases upon the solvent molecules. As a result, they demonstrated high-performance ambipolar perovskite FETs that exhibited mobilities greater than 10 cm^2 V^{-1} s^{-1} at room temperature. Representative (I_D–V_{GS}) characteristics for both hole and electron transports in the saturation regime (drain–source voltage, $V_{DS} = \pm40$ V) are shown in Fig. 11d(iii) and (iv), respectively.[170]

Overall, any strategy that can minimize charged point defects located at the GBs, decrease polarization fluctuations of the ions with larger grains and optimize contact to induce highly crystalline order, as well as isolate the source–drain electrode from the perovskite, can be effective in fabricating efficient FET devices. Certainly, mono-HPs with extremely low defect density, high mobility, independence from GBs, and higher structural order form a better platform. However, corresponding investigations based on mono-HP FET devices have been rarely reported. Until recently, Li *et al.*[166] reported a FET based on $MAPbI_3$ mono-HP microplates. They grew mono-HP microplates adopting a method of patterned growth of regular arrays of perovskite microplate crystals.[171] Meanwhile, they also incorporated the mono- and bilayer graphene stripes as source–drain contact electrodes for mono-HP FETs, for not only tuning the barrier height at the interface of graphene/mono-HPs but also reducing the contact profile to enable the fabrication of a smooth device capable of being fully encapsulated by a boron nitride (BN) layer for higher device stability (Fig. 12a(i)). By examining the field effect, they found that the temperature could modulate the doping type of $MAPbI_3$ mono-HPs. At lower temperatures, the material exhibited p-type behavior, which gradually diminished when the temperature increased and finally vanished at around 180 K (Fig. 12a(iii)). At lower temperatures (2 K), the p-type behavior was retained and the source–drain current continuously increased with decreasing temperatures, as shown in Fig. 12a(iv)).[166] It should be noted that as the device is built upon mono-HP crystals, the electron mobility determined from such FET devices displays a large value of 4 $cm^2 V^{-1} s^{-1}$ at 77 K, which is dramatically larger than those in poly-HP FET devices. Yu *et al.*[71] demonstrated high-performance FET devices based on $MAPbX_3$ (X = Cl, Br, or I) mono-HPs with both BGTC and BGBC device configurations (Fig. 12b). The on/off current ratio ranging from 10^3 to 10^5 could be readily achieved at room temperature. These devices showed operating voltages lower than 5 V; in fact, the BCBG design exhibited the lowest voltages <2 V. The maximum room-temperature mobilities of 2.6–4.7 and 0.26–2.2 $cm^2 V^{-1} s^{-1}$ could be obtained for electron and holes, respectively. Interestingly, as the $MAPbCl_3$ has a wide bandgap, the device is almost transparent in the visible range, making it a promising candidate for applications in transparent and imperceptible electronics.[71] On the other hand, the form of mono-HP also enables people to understand its anisotropy in charge transport. For example, Lv *et al.*[172] constructed a $MAPbI_3$ mono-HP FET device (Fig. 12c(i)). They built a vertical-structured FET device using $MAPbI_3$ mono-HP with specific crystal directions (*i.e.*, [100], [112], and [001]) parallel to the out-of-plane direction of the device and investigated its ambipolar field-effect



	[100]	[112]	[001]
$\mu_e / cm^2 V^{-1} s^{-1}$	3.41×10^{-4}	2.83×10^{-4}	1.82×10^{-4}
$\mu_h / cm^2 V^{-1} s^{-1}$	5.45×10^{-4}	5.55×10^{-4}	2.80×10^{-4}

Fig. 12 Mono-HP FETs. (a) Schematic of the back-gate, back-contact $MAPbI_3$ mono-HP FET built on a 300 nm SiO_2/Si substrate with monolayer graphene as the contact, covered by a BN layer (i). The optical image of the BN-covered device with graphene (red dashed line), perovskite (black dashed line), and BN (dark yellow dashed line) highlighted by different color lines. The mono-HP thickness is ~150 nm (ii). The temperature-dependent transfer characteristics in the low-temperature (iii) and ultralow-temperature (iv) ranges.[166] Copyright © 1999–2019 John Wiley & Sons, Inc. (b) Schematic representation of a bottom-gate, bottom-contact FET device (i). The mono-HP is $MAPbX_3$ (X = Cl, Br, or I). A representative transfer characteristic of $MAPbCl_3$ mono-HP FET device (ii) using forward/reverse gate voltage sweeps from −10 to 10 V at the rate of 0.05 V s^{-1}, where $V_{DS} = -2$ V. Inset: the linear regime of the respective devices. Field-effect hole mobility distribution for 20 devices fabricated and tested for each HP (iii).[71] Copyright © 2018, Springer Nature. (c) Sketch of a vertical-structured mono-HP FET of $MAPbI_3$ (i). Views of the crystal structure along the [100], [112], and [001] orientations and the corresponding FET mobilities for each direction (ii).[172] © Copyright 2019 IEEE.

characteristics in the dark along these directions. As compared to the [100] and [112] orientations, charge carriers have lower mobility along the [001] direction.[172] Certain materials exhibit birefringence, which differentiates the moving speed of photons along the different directions in crystals. This birefringence can be used for time-resolved double-slit experiments with entangled photons.[173] Analogously, the electrical anisotropy in mono-HPs might be a good platform for similar time-resolved double-slit experiments involving electrons.

5.2 $CsPbX_3$ mono-HP-based FETs

Earlier, we discussed ion migration issues in most $MAPbI_3$-based HP FETs. However, besides the low activation energy of MA^+ from the lattice, an organic cation is also sensitive to moisture and heat. Comparatively, replacing the A-site organic cation with inorganic alkalis can provide stronger moisture and thermal stabilities. Considering the ion size as well as tolerance factor[174] that describes the geometric stability of the crystal lattice, $CsPbX_3$ represents the principle inorganic perovskite material for optoelectronic applications.[175–177] Meanwhile, several other HPs, *e.g.*, $Cs_x(MA_{0.17}FA_{0.83})_{1-x}Pb(Br_{0.17}I_{0.83})_3$,[160] using mixed components have also been reported. For example, Huo *et al.*[178] reported $CsPbBr_3$ mono-HP-based FETs (Fig. 13a(i) and (ii)). A $CsPbBr_3$ mono-HP microplatelet was obtained by VDW epitaxy, and it was transferred to the FET substrate using the pick-up method (with no liquid involved); hence, there was no surface damage to the platelets. Field-effect hole mobility (μ_h) of 0.3 $cm^2 V^{-1} s^{-1}$ and on–off ratio of 6700 at room temperature, as well as μ_h of 1.04 $cm^2 V^{-1} s^{-1}$ and on–off ratio $>10^4$ at 237 K, could be obtained (Fig. 13a(iv)). The mobility in $CsPbBr_3$ mono-HP FETs is still determined by the interaction between the charge carriers, ions, and phonons at the semiconductor–dielectric interface. However, ion migration plays an important role in the electrical transport process at relatively higher temperatures (above $\sim$237 K); further, the interaction between charge carriers and phonon scatterings dominates at lower temperatures (below $\sim$237 K). The $CsPbBr_3$ mono-HP devices also displayed one-month ambient stability, owing to the material's intrinsic robust stability in addition to the potential functionality of the polyvinyl alcohol (PVA) film coated outside the perovskite.[178] In addition, they further constructed a heterojunction of mono-HP and traditional 2D materials such as graphene, MoS_2 (Fig. 13b(i)), and hexagonal BN (h-BN).[179] Such a $CsPbBr_3$ mono-HP/2D material (graphene, MoS_2, and h-BN) heterostructures were achieved by VDW epitaxy.[178] As MoS_2 exhibits the best energy level alignment with $CsPbBr_3$ mono-HPs, $CsPbBr_3/MoS_2$ heterojunction FET (Fig. 13b(ii)) exhibits the best device performance in this study. Using a channel length of 100 μm, the FET exhibits hole mobility of 0.08 $cm^2 V^{-1} s^{-1}$ in the dark and that of 0.28 $cm^2 V^{-1} s^{-1}$ under 442 nm laser illumination at an intensity of 0.2 mW cm^{-2} driven by a low voltage of 0.5 V at room temperature in ambient air. Such a VDW heterojunction of perovskite/2D material combines the excellent properties of both perovskite and 2D materials and reduces the resistance loss into heat because of a minimized Schottky barrier, which may help to minimize the device size and corresponding power dissipation.[179] In addition, $CsPbX_3$-based quantum dot (QD) materials that are nanometer sized or smaller and coated with organic ligands have also been employed in the FET, particularly for LED applications. The confinement energy in smaller QDs due to the split in the energy levels increases the total emission energy and emissions at various wavelengths. Further, the organic ligands are supposed to protect the QDs against moisture. Such HP-QD light-emitting FETs have been reported in the field of quantum LEDs (QLEDs), QD displays, *etc.*[180–182] Beyond these 0D (QD) and 2D (microplate) mono-HPs, one-dimensional (1D), *i.e.*, nanowire (NW) HP, is another type of material for FET applications. In particular, 1D HPs have been demonstrated to exhibit many interesting properties, attracting various potential applications, such as optical communication, computing, imaging, Fabry–Perot cavity, and gain medium for optical amplification.[183–186] Recently, Meng *et al.*[187] developed a $CsPbX_3$ 1D mono-HP FET device. They employed the catalytic vapor–liquid–solid (VLS) growth method for growing $CsPbX_3$ 1D NWs. Fig. 13c(i) shows the schematic illustration of the VLS growth process of $CsPbX_3$ NW (X = Cl, Br, or I) using Sn catalysts. The SEM image of vertical $CsPbBr_3$ NWs grown on SiO_2/Si substrates and tilted SEM images of different individual $CsPbBr_3$ NWs grown with Sn catalytic seeds are shown in Fig. 13c(ii). A FET device is constructed by bridging the $CsPbBr_3$ NW between two electrodes (Fig. 13c(iii)). The corresponding transfer characteristics using the logarithm of the *y*-coordinate is shown in Fig. 13c(iv)). Upon illumination in the visible regime, $CsPbX_3$ 1D mono-HP opto-FET devices exhibit responsivity exceeding 4489 A W^{-1} and detectivity over 7.9×10^{12} Jones. A dark FET exhibits superior field-effect mobility of 3.05 $cm^2 V^{-1} s^{-1}$ at room temperature. The VLS-grown perovskite NWs seem to be versatile platforms for exploring the fundamentals and potential applications on the basis of 1D mono-HPs.[187]

5.3 Quasi-2D mono-HP-based FETs

Compositionally, the prototype HP has the chemical formula ABX_3, where A denotes small organic cations and/or alkali metal cations (such as Cs^+), B denotes bivalent metals (such as Pb^{2+} and Sn^{2+}), and X is a halogen. The size of the ions at each crystallographic site needs to accommodate the tolerance factor,[174] $t = (r_A + r_X)/\sqrt{2}(r_B + r_X)$, where r_A, r_B, and r_C denote the radii of ions at the A-, B-, and X-sites, respectively. As t gets close to 1, the crystal maintains a 3D structure; however, as r_A increases, t becomes larger than 1 and the crystal will have lower structural dimensionality, such as that in layered two-dimensional (2D) HPs. The 2D HP has the generic formula $(RNH_3)_2(CH_3NH_3)_{n-1}B_nX_{3n+1}$, where R is an alkyl or aromatic moiety, B is a metal cation, and X is a halide.[6] An organic layer consists of a large organic moiety, namely, RNH_3^+, which is typically insulating and plays the role of a barrier layer, while the inorganic layer, namely, $[(CH_3NH_3)_{n-1}B_nX_{3n+1}]^{2-}$, is semiconducting in nature. As the thickness of each layer is scaled down to the angstrom and nanometer levels, quantum effects take place in these 2D HPs. Hence, the 2D HP structure is also termed as a MQW structure, as shown in Fig. 14a. The inorganic

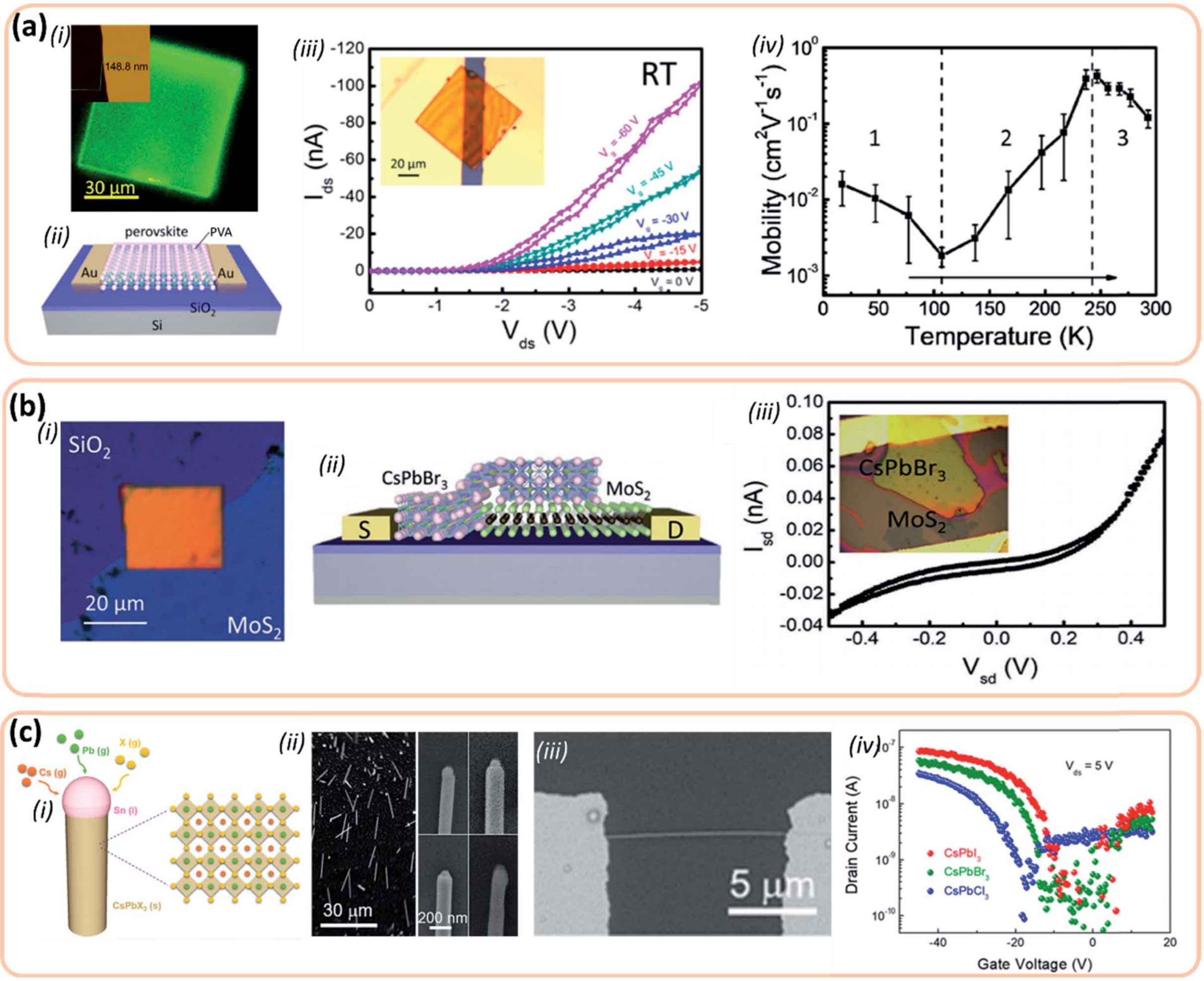


Fig. 13 $CsPbX_3$ mono-HP FETs. (a) FET based on VDW-grown and dry-transferred $CsPbX_3$ mono-HP ultrathin platelets. Photoluminescence image of a $CsPbBr_3$ mono-HP ultrathin platelet; inset: AFM image showing the cross-section profile (i). Output characteristic of $CsPbBr_3$ mono-HP FETs at room temperature; inset: an optical image of the FET device (ii). Temperature dependence of FET mobility (iii).[178] Copyright © 2017 American Chemical Society. (b) FET based on $CsPbBr_3$/2D crystal VDW heterojunctions. Optical images of typical $CsPbBr_3$ thin platelets on MoS_2 (i). Schematic illustration of a $CsPbBr_3$ mono-HP/MoS_2 heterojunction FET (ii). I_{sd}–V_{sd} curves of the heterojunction in darkness; inset: an optical image of the corresponding device (iii).[179] Copyright © 1999–2019 John Wiley & Sons, Inc. (c) 1D NW $CsPbX_3$ mono-HP FET. Schematic diagram showing the VLS growth process of $CsPbX_3$ NWs (X = Cl, Br, or I) using Sn catalysts (i). SEM and tilted SEM image of $CsPbBr_3$ NWs (ii). SEM image of the as-fabricated NW FET (iii). Transfer characteristics of the typical single VLS-grown $CsPbX_3$ (X = Cl, Br, or I) NW FETs using the logarithm of the *y*-coordinate (iv).[187] Copyright © 2019 American Chemical Society.

layer comprises the quantum well, which confines the charge carriers in the inorganic plane by quantum and dielectric confinement.[188] Hence, typically, 2D HP is not a good material for use in solar cells, as the photogenerated electron–hole pair is strongly connected with a large exciton binding energy (up of 0.5 eV),[189] which is dramatically higher than the thermal energy at room temperature (0.025 eV). Moreover, a 2D HP has an anisotropic charge transport property. In the out-of-plane direction, the organic insulating layer can block the charge transport, and the quantum tunneling probability is fairly low. In the in-plane direction, the charges are easier to move within each inorganic plane such that the magnitude of the in-plane electrical conductivity is higher than that of the out-of-plane one.[6] For example, for BA_2PbI_4 2D HPs, the in-plane hole mobility is 8.2×10^{-2} cm^2 V^{-1} s^{-1}, which is over one order of magnitude higher than the out-of-plane mobility (4.7×10^{-3} cm^2 V^{-1} s^{-1}).[6] Hence, taking advantages of such an anisotropic transport property, 2D mono-HP FET devices can be of considerable interest.

2D HP materials have been employed into FET applications since early times. For example, by replacing the A-site cation with large aromatic and aliphatic cations, 2D HPs, such as phenylethyl ammonium tin iodides ($(PEA)_2SnI_4$) or ($(C_6H_5C_2H_4NH_3)_2SnI_4$)[190,191] and alkyl ammonium tin iodides ($(C_nH_{2n+1}NH_3)_2SnI_4$ (n = 4–12)),[192] have been introduced into FETs. Notably, $(PEA)_2SnI_4$ (ref. 193) was the first HP material to be utilized in a FET device, which was initially intended for channel materials. The reported field-effect mobility of ($C_nH_{2n+1}NH_3)_2SnI_4$ (n = 4–12) is very low (~10^{-3} to 10^{-2} cm^2 V^{-1} s^{-1}). Recently, Matsushima *et al.*[194] demonstrated a record μ_h

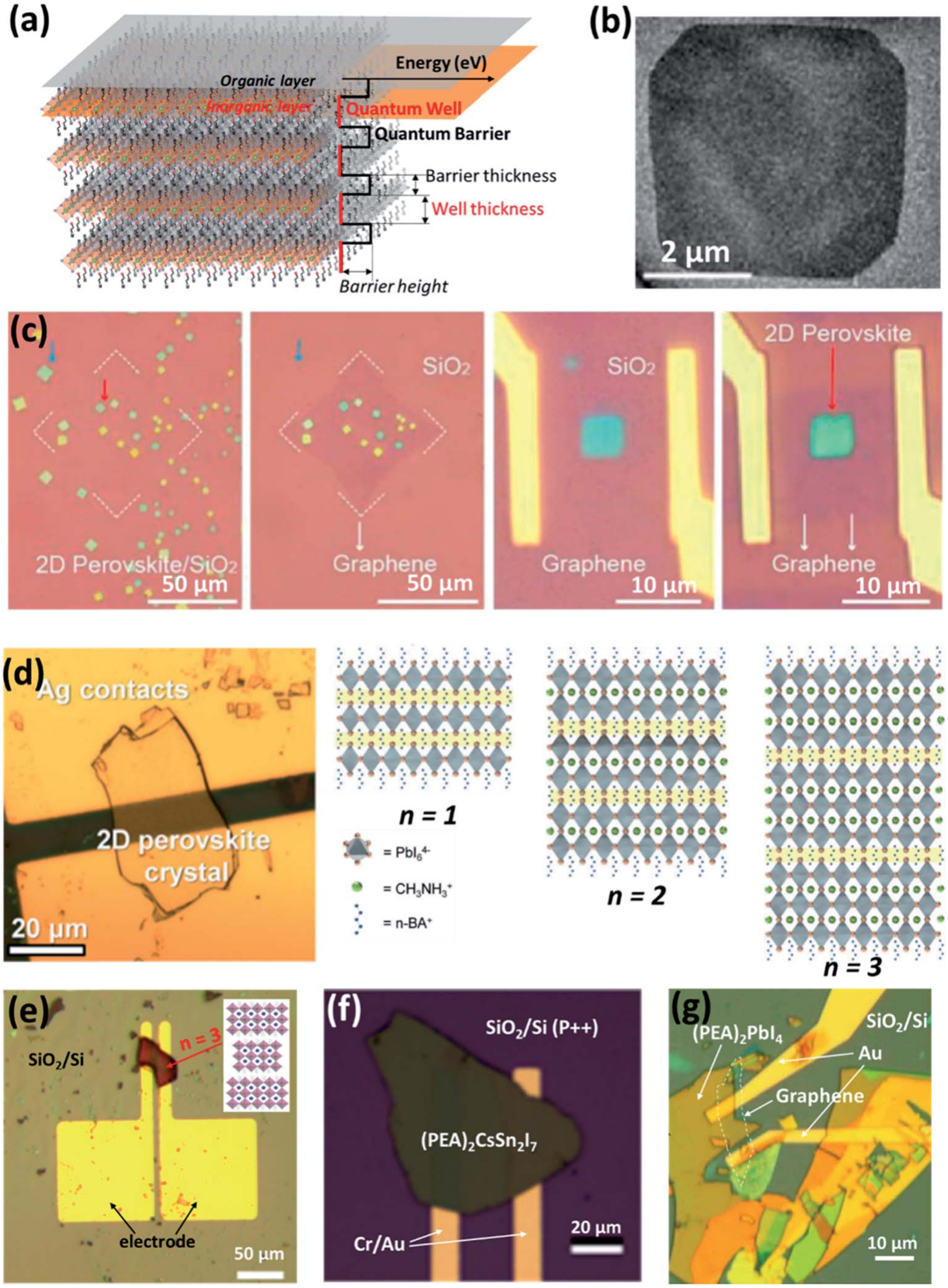


Fig. 14 2D mono-HP-based FETs. (a) A general molecular structure of a 2D mono-HP material, showing the MQW structure with an energy diagram revealing the organic layer as the quantum barrier and inorganic layer as the quantum well layer. (b) and (c) $(C_4H_9NH_3)_2PbBr_4$ 2D mono-HP and FET. (b) Low-magnification TEM image of a $(C_4H_9NH_3)_2PbBr_4$ 2D mono-HP. (c) From left to right: optical images of $(C_4H_9NH_3)_2PbBr_4$ 2D mono-HP grown on 300 nm SiO_2/silicon substrate before and after the dry transfer of the graphene film. Within the white dotted line, the 2D crystals are covered by a graphene film, whereas the outside area remains uncovered. Optical images of graphene-protected $(C_4H_9NH_3)_2PbBr_4$ 2D mono-HP before cutting out a channel and after installing graphene electrodes.[199] Copyright © 2016 American Chemical Society. (d) Optical image of the exfoliated $(BA)_2(MA)_{n-1}Pb_nI_{3n+1}$ 2D mono-HP with Ag contacts, with the schematic illustration of the 2D mono-HP of different quantum well layer thicknesses, *i.e.*, $n = 1$, 2, and 3.[200] Copyright © 1999–2019 John Wiley & Sons, Inc. (e) Optical image of a FET device based on $(BA)_2(MA)_{n-1}Pb_nI_{3n+1}$ ($n = 3$) 2D mono-HP plates with a thickness of around 20 nm.[96] Iop Publishing, Ltd. (f) Optical image of a FET device based on $(PEA)_2CsSn_2I_7$ 2D mono-HP.[201] Copyright © 2018 American Chemical Society. (g) Optical image of a FET device based on $(PEA)_2PbI_4$ 2D mono-HP.[204] © 2018 Elsevier Inc.

value of up to 15 $cm^2\ V^{-1}\ s^{-1}$ for $(PEA)_2SnI_4$ at room temperature by resolving the aforementioned issues of low perovskite quality, high carrier trap density, and inefficient carrier injection, *via* the surface treatment of the substrate with a self-assembled monolayer in combination with the adoption of a top-contact/top-gate (TC/TG) structure with hole-injection layers. Further, field-effect electron mobility (μ_e) of 2.1 $cm^2 V^{-1} s^{-1}$ was reported for this 2D $(PEA)_2SnI_4$ poly-HP thin film.[195] It should be noted that $MASnI_3$ mono-HP has been observed to have ultrahigh mobility of 2320 $cm^2 V^{-1} s^{-1}$, which is significantly higher than its poly-HP thin-film counterparts.[196] Hence, $(PEA)_2SnI_4$ mono-HP is also expected to have extra room for higher mobilities.[194] However, most Sn-2D HP FETs are built upon poly-HP thin films using the spin-casting method for sample preparation, and their monocrystalline devices are rarely reported due to the instability of Sn-2D HP materials (Sn^{2+} in Sn-2D HP can be easily oxidized into Sn^{4+}). Comparatively, Pb-2D HP materials tend to have higher ambient stability.[197] So far, most studies involving Pb-2D HP materials have concentrated on poly-HP thin films, while there are limited reports focusing on ultrathin 2D mono-HP-based FETs.[166,171,198] Only a few photoresponse FETs based on 2D mono-HPs have been reported. For example, Tan *et al.*[199] demonstrated the first 2D mono-HP-based photodetectors with a FET structure, assisted with the protection and electric contact of monolayer graphene. Fig. 14b shows the low-magnification TEM image of a thin $(C_4H_9NH_3)_2PbBr_4$ crystal at the micrometer scale. These devices show promising optoelectronic properties, such as high current on–off ratio up to 10^3 and low dark current of $\sim 10^{-10}$ A, yielding high photodetection efficiency. In particular, they used a submillimeter-sized single-crystal graphene film as the medium to convey the as-synthesized 2D perovskite crystals onto the channel between the two electrodes of the FET device (Fig. 14c). Another well studied material, $(BA)_2(MA)_{n-1}Pb_nI_{3n+1}$, known as a Ruddlesden–Popper (RP) HP, has also been investigated for use in FETs. Li *et al.*[200] demonstrated a series of 2D mono-HP FETs based on high-quality exfoliated 2D $(BA)_2(MA)_{n-1}Pb_nI_{3n+1}$ crystals with varying n values (Fig. 14d) under different temperatures. They found that unipolar n-type transport dominated the electrical properties of all these $(BA)_2(MA)_{n-1}Pb_nI_{3n+1}$ 2D RP mono-HPs. The transport behavior exhibits strong dependence on the n value; further, the mobility substantially increases as n increases. The corrected FET mobility values for $n = 1$, 2, and 3 are 2×10^{-3}, 8.3×10^{-2}, and 1.25 $cm^2 V^{-1} s^{-1}$ at 77 K, respectively. In addition, by correlating the temperature-dependent electrical transport and optical measurements, it is found that the origin of carrier mobility dependence on the phase transition is different between 2D and 3D mono-HPs.[200] Li *et al.*[96] also constructed their FET on the basis of the same $(BA)_2(MA)_{n-1}Pb_nI_{3n+1}$ 2D RP mono-HPs. Fig. 14e shows the optical image of a FET device based on $(BA)_2(MA)_{n-1}Pb_nI_{3n+1}$ ($n = 3$) 2D mono-HP plates. In particular, they also controlled the phase purity by the mechanical exfoliation method. Using this exfoliation method, 2D mono-HP microplates with a thickness of around 20 nm could be obtained, which yields several repeating unit layers in such mono-HPs. By integration with other 2D layered materials (such as BN) and getting transferred to prefabricated electrodes, photoresponsive FET devices can be obtained.[96] In addition, FETs using 2D mono-HP materials with different large organic cations at the A-site have also been investigated. For example, Shen *et al.*[201] reported a new type of 2D lead-free mono-HP, namely, $(C_6H_5C_2H_4NH_3)_2CsSn_2I_7$, with millimeter size and high field-effect hole mobility. They used X-ray diffraction and low-temperature photoluminescence studies to verify the crystalline quality and phase purity, and energy-dispersive spectrometry measurements were used to confirm the presence of elemental Cs but the absence of Sn^{4+} (usually, Sn^{2+} can be easily oxidized into Sn^{4+}; therefore, the absence of Sn^{4+} indicates high material purity). Using the as-synthesized 2D mono-HP, high electrical conductivity and high hole mobility (up to 34 $cm^2 V^{-1} s^{-1}$ at 77 K) could be achieved. In terms of photoresponse, the corresponding FET device (Fig. 14f) also exhibits good performance, owing to the excellent optical properties and high electrical conductivity of 2D mono-HPs. Further, it should be noted that the reported $(C_6H_5C_2H_4NH_3)_2CsSn_2I_7$ mono-HP is free of elemental lead, suggesting a less-risk material for optoelectronic applications.[201] So far, 2D mono-HP FETs have shown promising charge carrier mobility values; further, due to the incorporation of large hydrophobic organic cations, 2D mono-HPs are expected to have greater stability.[202,203] Recently, Zhao *et al.*[204] revealed the spontaneous iodide loss process in 2D mono-HPs, which acts as an important degradation pathway of the crystal, inducing n-type doping of the perovskite semiconductor by generating positively charged iodide vacancies. Moreover, they demonstrated that covering 2D mono-HPs with graphene could sufficiently suppress this iodide loss, significantly improving the perovskite stability. Fig. 14g shows the photo-FET with a graphene/2D mono-HP/graphene structure, which shows no degradation for 75 days. This, together with the above studies from different groups, implies that the design using 2D mono-HPs onto other conventional 2D materials (such as graphene and BN) can be a promising sensitive diagnostic tool for fabricating stable and efficient FET devices.

5.4 Future of mono-HP FETs

The outstanding electronic structure of HP materials allows them to possess excellent electronic properties, such as large intrinsic charge carrier mobilities and ambipolar conductivity. These characteristics have imparted success in applications such as solar cells, with some figure-of-merit values approaching or even surpassing those of Si- or organic-semiconductor-based counterparts. Mono-HPs can be designed to exhibit features such as ultralow trap density, larger charge carrier diffusion length, longer carrier lifetimes, higher stability, *etc.* Currently, state-of-the-art FET devices based on HP materials still have issues such as intrinsic ion migration and hence induced ion-screening effects. Mono-HPs with reduced GBs and lower concentration of polar mobile ions, as well as 2D mono-HPs with minimized ion migration probability, can provide good platforms for mitigating such screening effects. The strong optical response of mono-HP materials coupled with novel FET designs can provide newer opportunities for launching a new wave of research efforts in terms of novel integrated on-chip light sources, wave guides, phototransistors, and electrically pumped semiconductor lasers. The ion-based optoelectronic behavior can also trigger applications such as memristors,[97,205] artificial synaptic connections,[206,207] *etc.* Rapid progress is being made in developing growth techniques for mono-HPs, scalable processing of mono-HPs, and improving FET performance. Therefore, it is expected that many of the abovementioned materials and device issues will be resolved in the near future. Further, many new applications will be developed in related fields such as microprocessors, chip industry, complementary metal–oxide–semiconductor (CMOS) processing, *etc.*

6. Outlook

Single crystals are a highly appealing platform for investigating the fundamental, intrinsic, and natural properties of a material. Mono-HPs offer the potential to significantly enhance our understanding of the fundamental nature of materials by removing factors such as GBs, defects, and disordered morphologies. Mono-HPs provide a pathway toward achieving ultrahigh device performance due to the reduced energy losses through these imperfections. The compositional tunability of HP materials also enables the adjustment of multiple properties to satisfy specific application-platform-related requirements. Building upon the current understanding of HP materials, including an in-depth understanding of the basic materials' nature, various applications can be conceived that could not be considered earlier. The availability of single-crystal data can drive the development of theory and models in elucidating the underlying mechanisms controlling the physical response of such materials. This, in turn, can drive the design and development of synthesis techniques for mono-HP materials in order to achieve tailored responses for not only mono-HP PVs and FETs but also various other applications.

State-of-the-art poly-HP PVs have set the new PCE record (>25%). A straightforward projection suggests that the minimized Shockley–Read–Hall loss in mono-HP PVs could lead to superior efficiency than those obtainable using current poly-HP PVs, as well as a higher theoretically achievable PCE maximum value (30.5%). This implies that mono-HP PVs have the potential to outperform commercial Si PVs. Newly discovered nontrivial physics in mono-HPs, such as ferroelectric electron–hole channels, conductive edge states, photon recycling, and slower hot-carrier cooling phenomena, are shedding new light on the promise of PCE breaking through the Shockley–Queisser limit. The ongoing research on manufacturing of mono-HP wafers/thin films covering a variety of growth methods, such as floating, space-limited growth, VPE, and bulk-crystal slicing, are good examples of the possibility of fabricating materials with the desired quality and quantity to further explore these phenomena. In order to boost the PCE values of mono-HP PVs, several problems need to be resolved: (i) purity. Even though the HP material is expected to be defect-tolerant, a material with higher crystal phase purity can yield superior electrical properties. For example, efficient Si PVs require higher purity of Si (99.9999 wt%) to achieve reliable device efficiency. Taking into consideration the complex chemical-composition- and solution-based routes for the synthesis of HP materials, applying traditional purification processes are challenging, such as vaporization followed by chemical decomposition, to fabricate HP materials. The surface trap, morphological, and/or topographical control can present issues for mono-HP devices. (ii) Mechanics. HP materials are mechanically "soft" and "brittle". Typical processing techniques used for Si-based devices can damage HP materials. Therefore, specialized processes need to be developed for handling such HP materials. (iii) Stability. HP materials are very sensitive to the ambience, where moisture, heat, and radiation can cause damage. Therefore, dry rooms are required for quality control on the fabrication process of HP materials, as well as multifunctional coatings that can simultaneously improve the hydrophobicity and reduce surface traps. (iv) Toxicity. Mono-HP PVs consist of heavy metals that exhibit certain health concerns. Proper encapsulation can be fairly helpful at the device level, but contaminations occurring during material manufacturing and recycling need to be addressed. Material design based on ion exchange that provides a substitute for elemental lead with suitable nontoxic replacements can provide transformative progress. Reducing the thickness of mono-HPs and properly designing the device structure with efficient electron–hole extraction/blocking layers are important at the current stage of R&D involving mono-HP PVs.

Transistors and conductive lines are routinely fabricated upon silicon wafers to design electronic chips that drive our smartphones, laptops, and all other electronic gadgets. The manufacturing of typical chips and functional diodes is based on high-purity Si wafers that are processed using hi-tech, complex, and costly manufacturing processes. Industries have long sought cost-effective and alternative substrates on which the next generation of electronics can be built. Alternatives such as Si thin films and other semiconducting materials have been attempted for manufacturing transistors and similar devices. However, the rather complicated manufacturing techniques are challenging, particularly that involving high vacuum conditions and high purity processes. In contrast, mono-HP materials processed using solution-based approaches are much simpler platforms. The success of mono-HPs in the field of solar cells shows promise in providing an alternative to Si in certain select applications. The design of HP PVs is maturing, and significant progress is being made in developing HP-based FETs. In FET devices, charge carriers need to travel at the micrometer scale; therefore, the transport properties of the channel material play a critical role. Considering the trap density, GBs, charge mobility, and diffusion length, mono-HP materials can be a promising solution. Current research on mono-HP FETs is at the beginning stage. The proof-of-concept mono-HP FET devices reported recently still require high voltage to drive the gate, which are much higher than those for practical FETs. Therefore, more research is needed in this area to advance the implementation.

In conclusion, mono-HP wafers/thin-film materials are potentially promising platforms for fabricating ultrahigh-performance PVs and FETs. However, continued research is needed to resolve the pending issues starting from the crystal growth process to device construction. There is great momentum in the community to continue advancing mono-HP PVs and FETs, and it has become imperative for research agencies and industry to preserve this excitement.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

Y. H. and D. Y. acknowledge the support from AFOSR Biophysics and Natural Materials programs through award number FA9550-18-1-0233. K. W. and S. P. acknowledge the support from Air Force Office of Scientific Research under award number FA9550-17-1-0341. K. W. also acknowledges the financial support from IEE Stewardship Seed Grant Program. C. W. acknowledges the financial support from the Office of Naval Research (I. Perez) through grant number N000141613043.

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