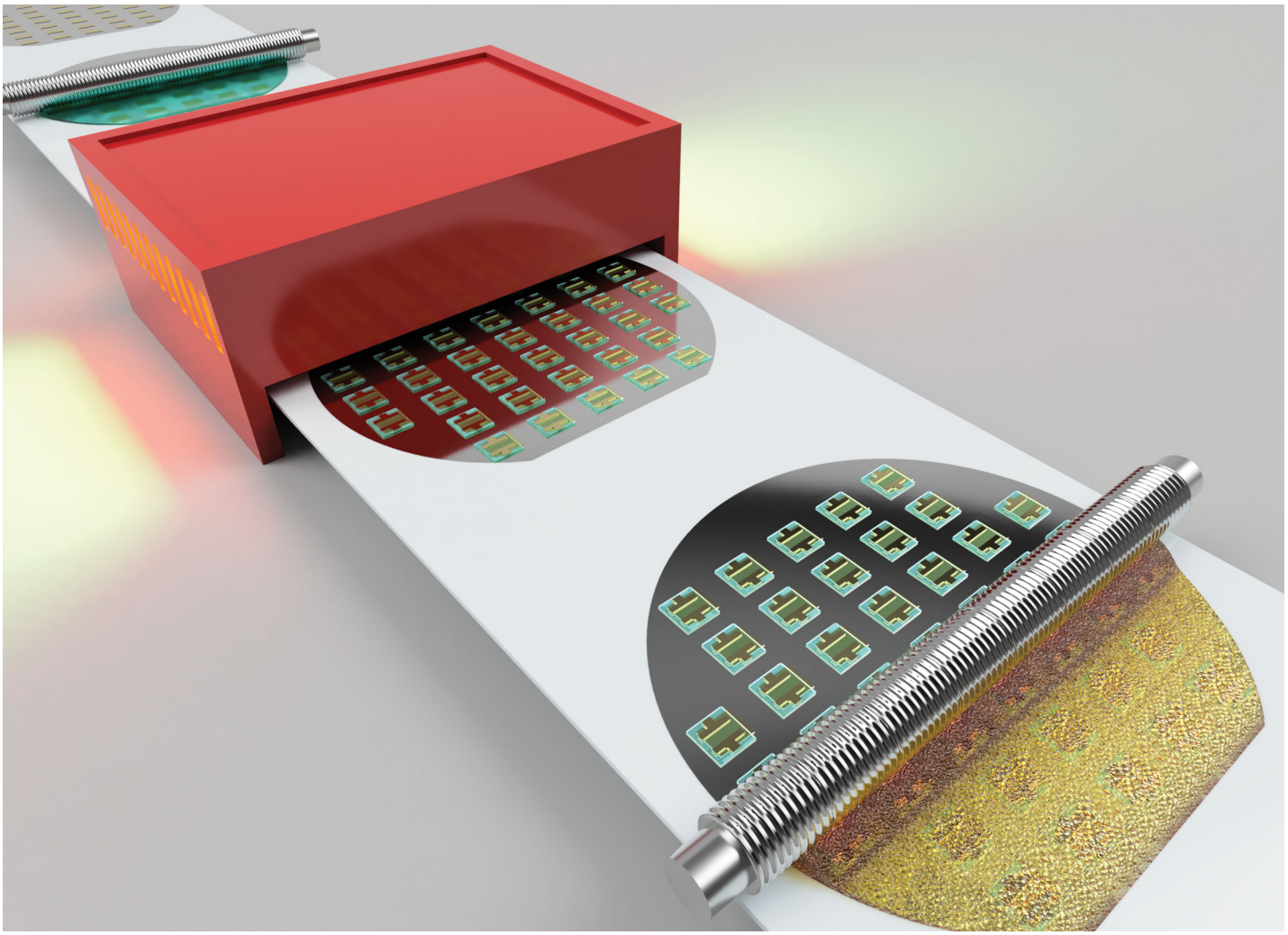

Showcasing research from Professor Myung-Han Yoon's laboratory, School of Materials Science and Engineering, Gwangju Institute of Science and Technology, Gwangju, Republic of Korea.

Large-area printed low-voltage organic thin film transistors *via* minimal-solution bar-coating

Large-area low-voltage OTFT arrays are fabricated *via* minimal-solution bar-coating. We investigated the effects of chemical composition and printing conditions on the cross-linked polyvinyl alcohol-based dielectric with good insulating properties and established its uniform deposition *via* bar-coating. Moreover, we demonstrated various aspects of large-area (up to 4-inch wafer) bar-coated cross-linked polymeric dielectric prepared from minimal solution (~1.2 μL cm^{-2}). A highly crystallized organic semiconductor layer was successively deposited on the polymeric dielectric layer *via* the minimum-solution bar-coating method, leading to the realization of large-area printed low-voltage organic transistor arrays.

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Large-area printed low-voltage organic thin film transistors *via* minimal-solution bar-coating†

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Herein, we report on the fabrication of large-area printed low-voltage organic thin film transistor arrays *via* minimal-solution bar-coating. We established the bar-coating of the chemically cross-linked polymer dielectric based on poly(4-vinylphenol) and 4,4′-(hexafluoroisopropylidene)diphthalic anhydride by investigating the effects of composition, reaction and printing conditions on film thickness, cross-linking efficacy, and dielectric properties. Subsequently, we elucidated various aspects of large-area (up to 4-inch wafer) bar-coated cross-linked polymeric dielectric prepared from minimal solution (~100 μL, ~1.2 μL cm^{-2}) by addressing film uniformity, thickness control, capacitance variation, underlying step coverage, patternability, *etc.* The resultant polymeric dielectric exhibited good insulating properties as exemplified by a low leakage current density of ~10^{-8} A cm^{-2} (at 1 MV cm^{-1}) and a high areal capacitance of 42.6 nF cm^{-2}. Finally, a highly-crystallized organic semiconductor layer based on 2,8-difluorinated 5,11-bis(triethylsilylethynyl)anthradithiophene was deposited on the bar-coated cross-linked polymeric dielectric *via* bar-coating, leading to the realization of printed low-voltage organic transistor arrays with minimum ink solution wasted.

Introduction

Recently, organic thin film transistors (OTFTs) have attracted considerable attention for their potential use in various functional electronics and displays.[1–6] The fundamental components of an OTFT are an organic semiconducting channel, a dielectric layer, and three metallic electrodes.[7] Consequently, the best performance of an OTFT can be achieved through the careful optimization of each component in terms of material, processing, and interfaces. Nonetheless, OTFT research has mainly focused on the development of high-performance organic semiconductors,[8–10] whilst the studies of various types and properties of dielectric materials still remain relatively less studied. The foremost challenge in optimizing the dielectric layer's performance in OTFTs is to identify the ideal combination of materials and processing that ensures both the enlarged capacitance and structural integrity that are necessary for low-voltage operation and minimum leakage current, respectively. Furthermore, the surface of the dielectric layer plays an important role in the bottom-gate structure, considering that the growth of an organic semiconductor channel and the charge transport at the interface are strongly influenced by the surface roughness and energy of underlying dielectric layer.

Chemical cross-linking significantly improves the solvent resistance and dielectric strength of polymers, without compromising their favorable processability.[11–13] Therefore, it is a particularly promising approach to incorporate polymeric dielectrics into printed organic electronics. Previously, Marks and coworkers demonstrated dielectric systems composed of several commonly-utilized polymers and trichlorosilane-based cross-linkers.[14,15] Moreover, Bao and coworkers formed dielectric networks from anhydrides or chlorosilane, and addressed their relevance to OTFT-based sensors.[16,17] Although these early reports and other research activities on cross-linked polymer dielectrics universally demonstrated their stable performance at low film thicknesses in nanoscale, the spin-coating has been predominantly employed for the deposition of polymeric dielectric films. Although the spin-coating offers the reproducible fabrication of uniform polymeric films regardless of semiconductors or dielectrics, the majority of materials is spun away during the film deposition, for example, more than 95% in the case of wafer-scale thin film coating.[18] Therefore, the substantial amount of precious materials (*e.g.*, semiconductors, dielectrics) and possibly toxic solvents (*e.g.*, halogenated solvents) are wasted, leading to the escalation in fabrication and waste-management cost. This situation becomes more serious in the case of processing large-area substrates.

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Bar-coating is a simple but scalable film deposition method for printed organic electronics.[19–26] Previously, we reported that the thickness of printed sol–gel metal oxide dielectric films can be controlled down to several nanometers by combining bar-coating with highly-diluted ink solutions, while the volume of dispensed solution on substrates is remarkably minimized (*e.g.*, ~100 μL for covering the whole 4-inch Si wafer).[25] Although several research groups made efforts to apply this promising printing method to the OTFT fabrication, they focused on either semiconductor or dielectric film deposition,[20–24,27,28] and there exist very few studies on the fabrication of large-area printed low-voltage OTFT arrays *via* minimal-solution bar-coating, which requires the optimization of both cross-likable dielectric and high-performance semiconductor deposition.

In this report, we report on the fabrication of large-area printed low-voltage OTFT arrays *via* minimal-solution bar-coating. We established the bar-coating of chemically cross-linked polymeric dielectric based on poly(4-vinylphenol) (PVP) and anhydride cross-linker by investigating the effects of composition, reaction and printing conditions on film thickness, cross-linking chemistry, and dielectric properties, which are supposed to be compatible with the ensuing semiconductor layer deposition. Subsequently, we elucidated various aspects of large-area (up to 4-inch wafer) bar-coated cross-linked polymeric dielectric using minimal solution (~100 μL, solution coating efficiency ~1.2 μL cm^{-2}) by addressing film uniformity, thickness control, capacitance variation, underlying step coverage, patternability, *etc.* Finally, highly crystallized organic semiconductor layer (2,8-difluorinated 5,11-bis(triethylsilylethynyl)anthradithiophene) (diF-TES-ADT) was deposited on bar-coated cross-linked polymeric dielectric *via* bar-coating, leading to the realization of large-area printed low-voltage OTFT arrays with minimum ink solution wasted.

Results and discussion

As shown in Fig. 1(a), we carried out the wire-wound bar-coating. The coating process proceeds in three steps: (i) dispensing the dielectric polymer solution onto the wire-wound bar, properly spaced, while maintaining a moderate gap distance (less than 100 μm) between the wire-wound bar and the substrate; (ii) moving the bar at a constant coating speed on top of the target substrate; (iii) gradually drying the deposited wet film

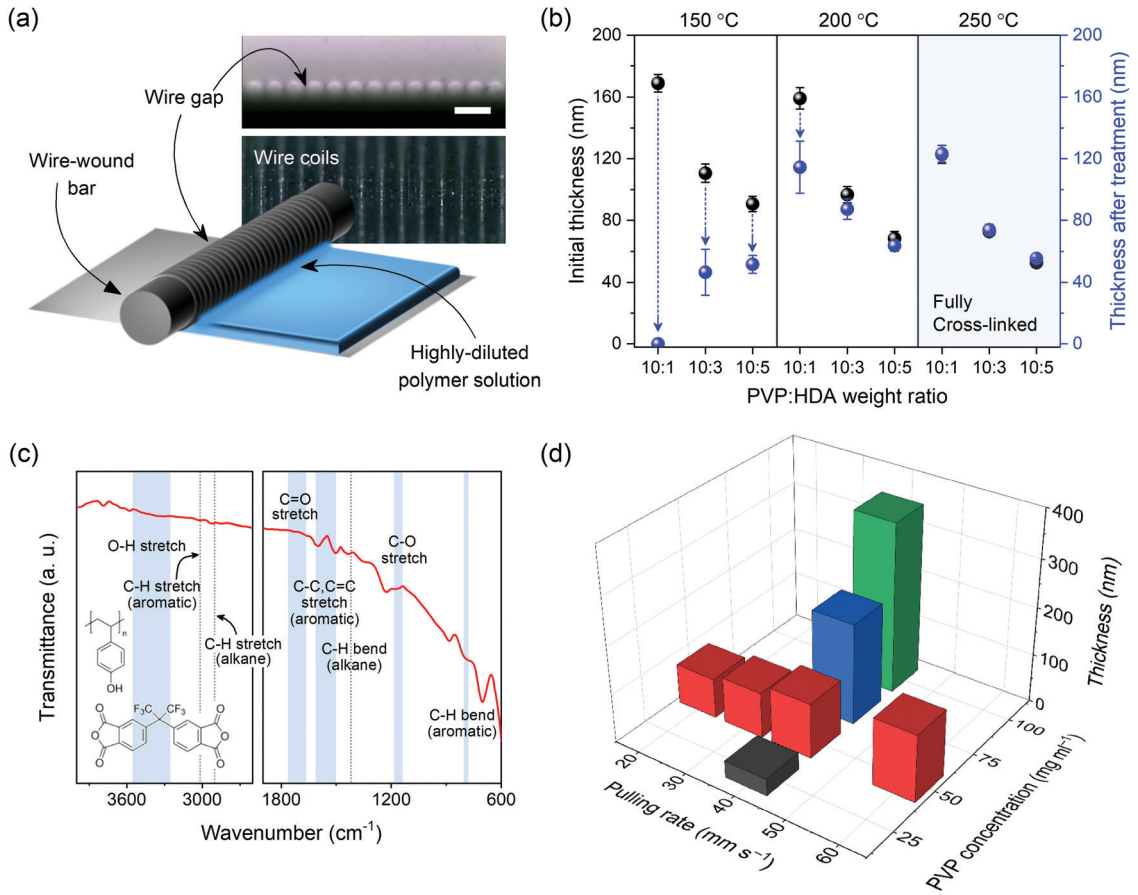

Fig. 1 (a) Schematic illustration and photograph of wired bar-coating (scale bar on the top image: 200 μm). (b) cPVP film thickness with various cross-linker contents (PVP : HDA weight ratio = 10 : 1, 10 : 3, and 10 : 5) annealed at different annealing temperatures (150, 200, and 250 °C). The initial film thickness and the final film thickness after solvent treatment are labeled with black and blue solid circles, respectively. (c) FT-IR spectra of a cPVP film. (d) Measured thickness map showing the controllability from the bar-pulling rate (20–60 mm s^{-1}) and solution concentration (25–100 mg ml^{-1}).

followed by the thermal annealing (see the details in the experimental section). Afterward, the solution trapped in the gaps between wires wrapped around the bar is merged by surface tension and spread evenly on the substrate due to the very diluted concentration, thus, sufficiently low viscosity, even when no thermal heating was applied to the underlying substrate during the film deposition.[29]

To realize the chemically and physically robust polymeric dielectric film *via* bar-coating, we selected 4,4′-(hexafluoroisopropylidene)diphthalic anhydride (HDA) as the crosslinker for PVP. Unlike silanes, HDA is chemically stable even in the presence of moisture which makes it ideal for ambient processing.[16] Furthermore, the cross-linking between anhydride and –OH in PVP does not generate toxic byproduct such as HCl. To identify the post-annealing condition in which the cross-linking reaction is pushed to the completion, we examined the solvent resistance of PVP–HDA-blended films before and after thermal annealing for 40 min at 150, 200, and 250 °C, while the weight ratio between PVP and HDA was varied (10 : 1, 10 : 3, and 10 : 5), yielding a total of nine combinations. The as-deposited and annealed films were immersed in the solvent used for solution preparation (*i.e.*, propylene glycol monomethyl ether acetate; PGMEA), and the film thicknesses before and after this treatment were measured by using a surface profiler. Fig. 1(b) shows that PGMEA visibly damages all the films annealed at 150 and 200 °C regardless of the cross-linking ratio as they experienced a reduction in thickness. In contrast, the cross-linked films annealing at 250 °C survived solvent test without any thickness reduction. Even with the lowest percentage of cross-linker (*i.e.*, 10% HDA), the degree of crosslinking increased and the corresponding film thickness reduction decreased gradually as the annealing temperature increased from 150 to 200 to 250 °C. We attribute the rather high annealing temperature to the absence of catalyst, and the annealing temperature could be reduced further by including catalyst and/or adding more cross-linker. Indeed, the results from higher HDA contents (30% and 50%) showed the improved film densification and chemical resistance due to the higher degree of chemical cross-linking inside PVP networks. But it is possible that the higher concentration of cross-linker may hamper the miscibility between PVP and solvent by inducing the microphase separation, resulting in the formation of pin-holes which are fatal to the insulating capability.[16,30] Therefore, we selected the PVP : HDA ratio of 10 : 1 and the post-annealing temperature of 250 °C for the rest of cross-linked PVP (c-PVP) film analysis and thickness control.

Fig. 1(c) shows the Fourier transform infrared spectroscopy (FT-IR) spectra of cPVP, in which the functional groups of both components are identifiable.[31] This implies that many chemical functionalities remained intact upon thermal cross-linking, while only reactive parts selectively attacked the neighboring functional groups to produce a solid physical network. Film solidification through bar-coating involves multiple processes which are dictated by mechanical interplay (*e.g.*, meniscus formation), thermal reflux, solvent drying, and surface energy. Hence, the bar-pulling rate and ink concentration are notably influential parameters that determine the final film thickness. As shown in Fig. 1(d), the thickness of cPVP increased monotonously from 30 to 350 nm at a constant bar pulling rate of 40 mm s^{-1} as the concentration of PVP increased from 25 to 100 mg ml^{-1}. In addition, the thin film became gradually thicker for higher coating speeds (from 20 to 60 mm s^{-1}) with the fixed polymer solution concentration of 50 mg ml^{-1}. These results demonstrate the outstanding ability of bar-coating to fine-tune the thickness of cross-linked polymeric dielectric film for specific applications. Such a delicate tunability of coated film thickness by increasing the polymer concentration and the bar-pulling rate, can be explained by the sufficiently low capillary number ($Ca = \mu v/\gamma$, μ: solution viscosity (N s m^{-2}), γ: solution surface tension (N m^{-1}), v: bar pulling rate (mm s^{-1})), in our case of the order of 10^{-3} ($Ca \ll 1$), followed by Landau and Levich regime.[19,22,25,32] (see the details in Fig. S1, ESI†). Considering that the surface tension is dominant over the low viscous force due to the high dilution, we suppose that the PVP–HDA-blended solution is ideal for achieving the reliable crosslinked polymer film deposition even at high coating speed.

The insulating properties of cPVP are of great importance for its use in potential device applications. Therefore, we fabricated metal–insulator–metal (MIM) devices and measured their leakage current and areal capacitance. The bar-coated cPVP films with the thickness of 63 nm exhibited a current density as low as 10^{-8} A cm^{-2} at an electric field of approximately 1 MV cm^{-1}, which is a significant improvement from pristine PVP thin films (Fig. S2, ESI†). Such a low range of leakage current density of the bar-coated cPVP film was also comparable to that of the spin-coated cPVP film while both films exhibited very low RMS roughness (0.19 and 0.18 nm). Intriguingly, we found that, after thermal annealing at 250 °C, the PVP only film exhibited good solvent resistance *via* self-crosslinking but poor insulating properties (Fig. S3, ESI†). This implies that the role of extra chemical cross-linker (*i.e.*, HDA) is critical for electrical insulation as well as solvent resistance by forming the dense network of polymer matrix within the solid film.

Despite the tremendous advantages of spin-coating such as simple processing, uniform film deposition, and facile thickness control, the majority of materials is wasted during the film deposition, resulting in the increase in both material and waste-management cost. This issue becomes more critical in the case of printing expensive synthetic semiconducting and/or dielectric polymers. Therefore, we investigated the application of bar-coating to the deposition of cross-linked polymer dielectric over large-area substrates, while the amount of used solution is minimized. Fig. 2(a) shows the photograph of the blended polymer solution bar-coated onto a 4-inch silicon wafer before thermal annealing, and the whole 4-inch wafer was divided into five sections starting from the region where the solution was initially loaded onto the wafer, for the purpose of analyzing film uniformity and device characteristics. As shown in Fig. 2(b), the bar-coated cPVP film exhibited relatively small variations in the film thickness (~200 nm), area capacitance (~22 nF cm^{-2} at 10 kHz), and dielectric constant (~5)

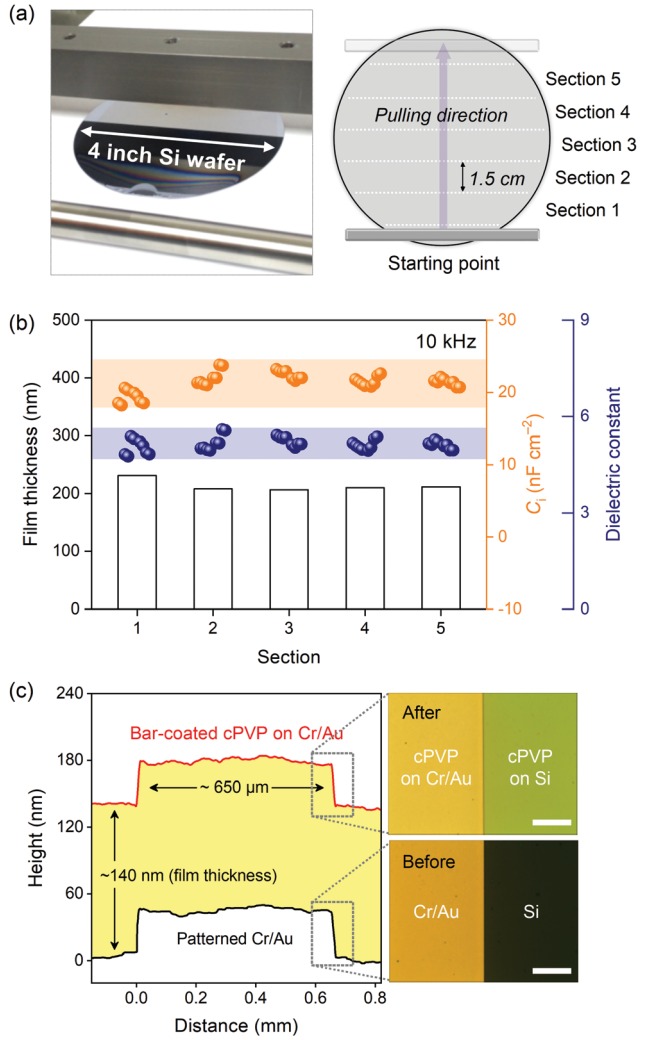

Fig. 2 (a) Photograph of the bar-coated precursor polymer solution on a 4-inch wafer (left). Graphical illustration of the geometrical sectioning of bar-coated wafer surface (right). (b) Physical and electrical characteristics of bar-coated cPVP film at different locations on a single 4-inch Si wafer. Vertical bars: film thickness, orange circles: C_i (capacitance per area at 10 kHz), blue circles: dielectric constant. (c) Surface profiles of the substrate (black) and the bar-coated cPVP thin film (red). The latter was vertically shifted by the film thickness. Right: Optical images showing the step edge before and after the film deposition (scale bars: 15 μm).

regardless of the distance from the initial bar-coating point. Such excellent uniformity across the whole wafer can be attributed to the guided solution spreading and stable drying process due to the uniform coating of highly diluted solution. More importantly, it is remarkable that only less than 100 μL of solution was employed to cover the entire 4-inch wafer substrate ($\sim$1.2 μL cm^{-2}), showing the similar film quality and uniformity but a potential advantage over spin-coating which typically requires at least $>$5 ml of solution to cover substrates with the similar areas.[23–25] Additionally, we confirmed that the bar-coated polymeric dielectric film conformally covered the underlying nanoscale features such as patterned metallic electrodes. Fig. 2(c) shows that the sharp side edges of a pre-patterned metal strip were not buried or flattened by the bar-coated cPVP film. We expect that this may be useful in applications where the structural replication is very important, for instance, optical gratings.

To integrate a dielectric material into functional electronic devices, it must withstand a diverse range of chemical processes for patterning spatial features and depositing additional layers atop. Therefore, to address this issue, we performed the conventional photolithographic patterning of Cr/Au on top of the bar-coated cPVP film (see the details on the photolithography process in the experimental section). As shown in Fig. 3(a), the whole procedure involves the wet-processing of photoresist (PR) film on top (*i.e.*, coating, backing, developing, removing, *etc.*) as well as the UV exposure, which may cause irreversible damage to the chemical and/or dielectric properties of the underlying polymeric film. Fig. 3(b) is an optical photograph of the patterned bar-coated cPVP film after the photolithographic procedure for the definition of source and drain electrodes followed by semiconductor deposition (*vide infra*), showing that the surface of cPVP remained intact at the macroscale. Atomic force microscopy (AFM) images were also obtained to detect any possible nanoscale changes in cPVP film after the photolithography process. Fig. 3(c) and Fig. S4 (ESI†) indicate that cPVP is remarkably resistant to the wet chemical processes involving PR developer (*e.g.*, aqueous alkaline solution), acetone, and other common solvents, as confirmed by the observation that its surface roughness (R_q) was almost identical after a series of chemical treatments: 0.23 (bare), 0.25 (MIF developer), 0.26 (acetone), 0.23 (PGMEA), 0.23 (tetralin), and 0.24 nm (chlorobenzene). Furthermore, Fig. 3(d) demonstrated that cPVP can be precisely patterned by combining the conventional photolithography with the dry gas etching, a finding that has direct implications for feasibility for adequate isolations among devices and *via*-holes in a layered circuitry.

Finally, we fabricated printed OTFT devices in the bottom-gate bottom-contact (BGBC) configuration by successively applying the bar-coating to both dielectric and semiconducting layers (Fig. 4(a)). Note that the BGBC geometry is desirable for many integrated circuits that require narrowly spaced electrodes and bus lines. Furthermore, to take full advantage of bar-coating for both the minimal usage of dielectric/semiconducting materials and the guidance of crystalline material growth, we employed 2,8-difluorinated 5,11-bis(triethylsilylethynyl)anthradithiophene (diF-TES-ADT) as an air-stable p-type semiconductor that features contact-induced crystallinity.[33,34] Briefly, the Au source/drain electrodes were patterned as described above and treated with the self-assembled monolayer (SAM) of pentafluorobenzenethiol (PFBT). Subsequently, diF-TES-ADT was bar-coated in the direction parallel to that of the drain current.[35] The polarized optical microscopy (POM) image (Fig. 4(b)) of the bar-coated semiconducting layer displays the characteristic templated growth of diF-TES-ADT molecules that nucleate on the fluorinated metal before extending towards the insulator region.[36] The underlying 97 nm thick cPVP thin film offered a reasonably enlarged capacitance (42.6 nF cm^{-2}), excellent electrical insulation, and efficient charge transport at the interface with the diF-TES-ADT layer. The representative output

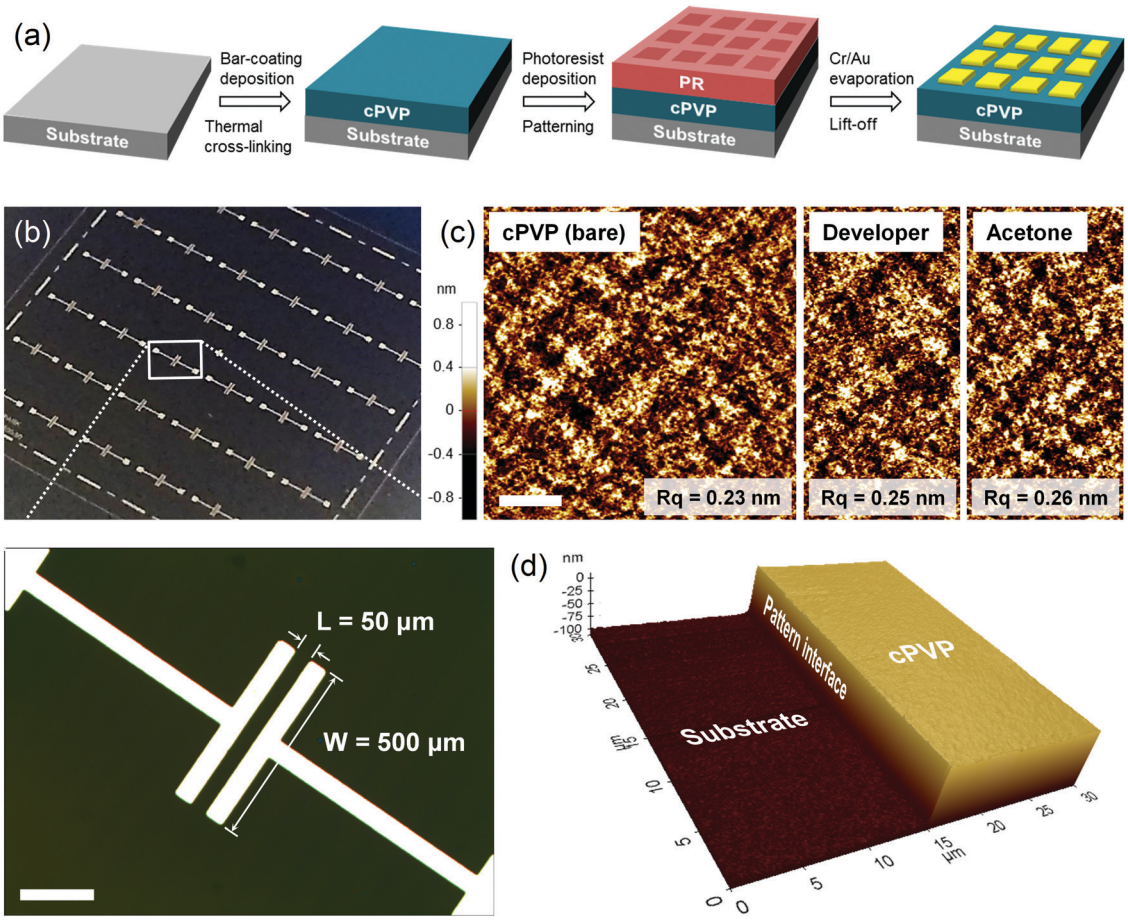

Fig. 3 (a) Schematic illustration of the photolithographic patterning of metal contacts on the cPVP thin film. (b) Photograph of the patterned transistor electrodes (*L*: channel length, *W*: channel width, scale bar in the zoomed-in image: 200 μm). (c) AFM height images showing the topography of the bare cPVP thin film and cPVP thin films after developer or acetone immersion (scale bar: 1 μm). (d) 3-D AFM reconstruction of a cPVP layer patterned by lithography and dry etching.

curves shown in Fig. 4(c) feature the complete switching under 10 V along with proper channel pinch-off. The field-effect mobilities of several devices were determined to be in the range of 0.1–0.2 $cm^2 V^{-1} s^{-1}$ (Fig. 4(d) and Fig. S5, ESI†). The prepared OTFT devices also exhibited the concurrent gate leakage currents as low as 100 pA and the source–drain current on/off ratios exceeding 10^4 (Fig. 4(d) and Fig. S6, ESI†). The abovementioned device performance clearly demonstrates that the quality of the bar-coated cPVP film was not deteriorated during a series of multiple wet/dry processing steps including the source/drain electrode definition, the solution-based SAM deposition, the numerous solvent rinsing, and the diF-TES-ADT bar-coating.

Conclusions

In summary, we successfully fabricated large-area printed low-voltage organic thin film transistor arrays *via* minimal-solution bar-coating. The detailed characterization of the cPVP thin films produced at different process parameters provided a general insight into the engineering of bar-coating and polymeric dielectric to incorporate chemically cross-linked polymeric dielectric to printed organic electronics. Furthermore, the recently emerging bar-coating process showed promising potential for creating thin films with precisely tailored physical dimensions with minimal material consumption particularly over large-area substrates. Considering that the bar-coating technique is comparable to more industry-friendly techniques such as roll-to-roll (R2R) slot-die coating, our cross-linked polymer dielectric recipe and low-temperature processing condition can be easily transferred to more practical large-scale printing methods. Furthermore, numerous favorable properties including high capacitance, strong chemical resistance, low leakage conduction at a reduced thickness, and smooth surfaces were achieved for the cPVP devices. The OTFTs prepared from bar-coated cPVP and diF-TES-ADT exhibited good performance at reasonably low applied voltages. This demonstrates that the presented procedure offers a promising strategy for enabling advanced large-area printed electronics.

Experimental

Materials

Poly(4-vinylphenol) (PVP, average $M_w \sim 25k$), 4,4′-(hexafluoroisopropylidene)diphthalic anhydride (HDA), propylene glycol monomethyl ether acetate (PGMEA), 2,3,4,5,6-pentafluorothiophenol

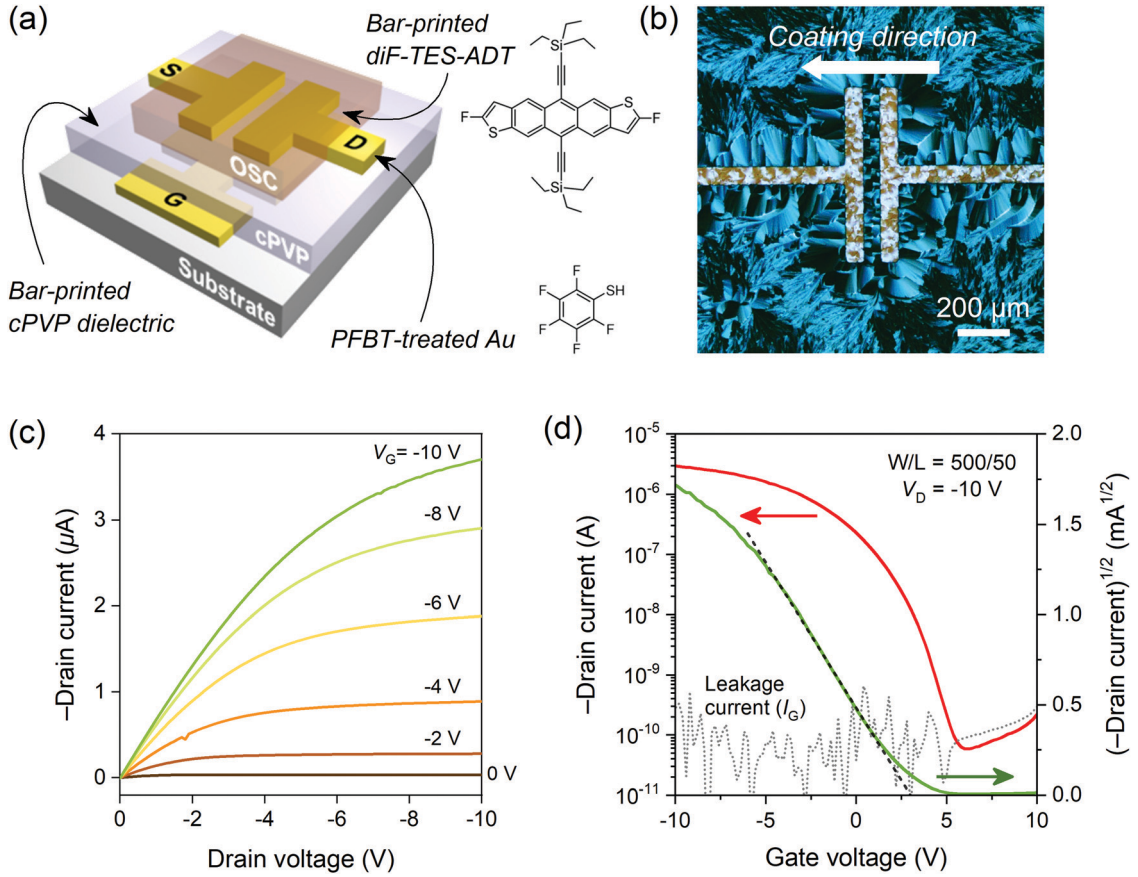

Fig. 4 (a) Structure of the OTFT fabricated by bar-coating of cPVP and diF-TES-ADT. Chemical structure of diF-TES-ADT (up) and PFBT (down). (b) POM image showing the surface microstructure of diF-TES-ADT domains. (c) Output (V_G: gate voltage) and (d) transfer characteristics (V_D: drain voltage) of the OTFT (W/L = 500/50 μm). The black and grey dotted line shows the region where the carrier mobility is extracted and the gate leakage current, respectively.

(PFBT), and toluene were purchased from Sigma-Aldrich. Isopropyl alcohol (IPA) was purchased from Merck Ltd. All materials were used without further purification. 2,8-Difluoro-5,11-bis(triethylsilylethynyl)anthradithiophene (diF-TES-ADT) was synthesized at the University of Kentucky.

Preparation of dielectric films

All substrates were cleaned by two successive sonication in acetone and IPA each for 10 min. Prior to the bar-coating, precleaned substrates were treated with oxygen plasma for 1 min immediately before polymer solution coating. We used a bar and wire coil which is commercially available with 1.3 cm and 100 μm dimeter, respectively (#4, RD specialties, USA). For the details on bar-coating process refer to the previous report.[25] The precursor polymer solutions were prepared by dissolving a 10 : 1 to 10 : 5 weight ratio of PVP and HDA in PGMEA. The concentration (25–100 mg ml^{-1}) of solutions was adjusted by PVP content. The solutions were filtered using a 0.2 μm polytetrafluoroethylene (PTFE) syringe filter and deposited at room temperature using a machine-controlled bar-coating system at a bar moving rate between 20 and 60 mm s^{-1}. The films were immediately soft-baked at 60 °C for 5 min, and annealed at 250 °C for 40 min to promote the cross-linking reaction. To fabricate the clean-edge stepped gate dielectric layer, the photoresist pattern was formed on the cPVP layer by the conventional lithography. Subsequently, the dry etching by plasma (50 W/air/40 sccm) is performed, followed by photoresist removal using acetone and IPA.

Preparation of bottom-contact electrodes by photolithography

A light-sensitive photoresist (PR, AZ GXR-601) was spin-coated on the deposited gate dielectric layer, exposed UV-light through a photomask, followed by development using the proper developer (AZ 300 MIF). For bottom-contact source and drain electrodes, 40 nm thick gold films with 3 nm thick chrome as an adhesive layer were deposited by thermal evaporation on the photoresist-patterned substrates. Finally, the photoresist was lifted-off using acetone and, then, the channel length (L) and width (W) as 50 and 500 μm were defined, respectively.

OTFT device fabrication

Au source/drain electrodes deposited on the bar-coated cPVP film were immersed in a 10 mM PFBT solution in IPA for 30 min for the deposition of SAMs, and rinsed with clean IPA and dried with nitrogen blowing. The diF-TES-ADT film was deposited using the solution of 2 wt% diF-TES-ADT in toluene

and the same bar-coater moved at 5 mm s^{-1}, while the substrate was heated at 70 °C. All the solution preparations and bar coatings were carried out under ambient conditions.

Film and device characterization

Thicknesses and morphologies of the dielectric films were measured by a surface profiler (Dektak XT, Bruker, USA) and a tapping-mode AFM (XE-Bio, Park Systems, Korea), respectively. Fourier transform infrared (FT-IR) spectroscopy was conducted using a Varian 660-IR model (USA). Regular optical images and POM images were taken using an Olympus BX51 model coupled with crossed-angle slit polarizers. Current–voltage characteristics of the OTFTs and capacitors were measured using a semiconductor parameter analyzer (Keithley 4200-SCS, USA).

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

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