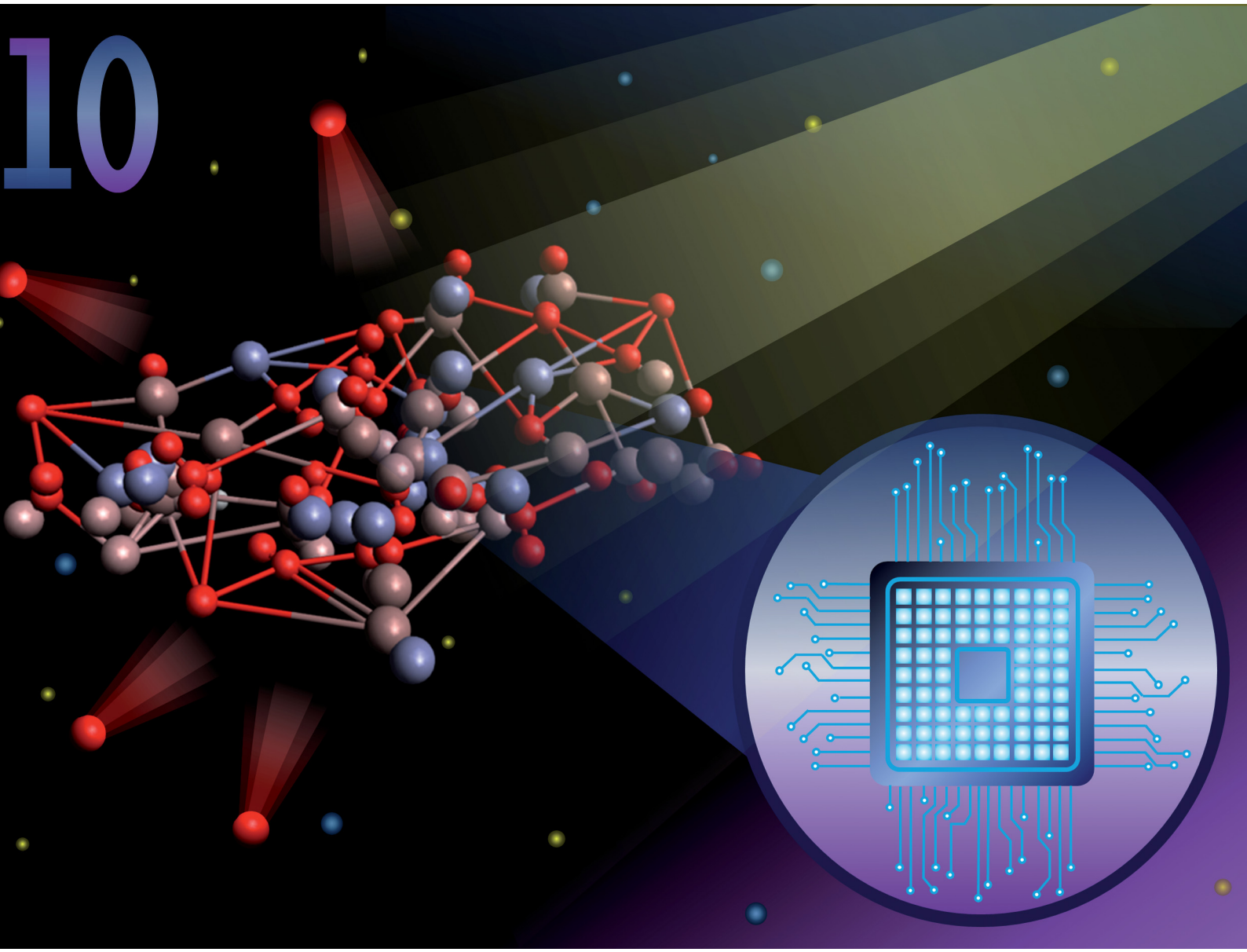
Volume 11
Number 22
14 June 2023
Pages 7109–7472

Journal of Materials Chemistry C

Materials for optical, magnetic and electronic devices

rsc.li/materials-c



ISSN 2050-7526

ROYAL SOCIETY OF CHEMISTRY

HIGHLIGHT
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Journal of Materials Chemistry C

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Cite this: J. Mater. Chem. C, 2023, 11, 7121

Enhancement of electrical stability of metal oxide thin-film transistors against various stresses

Youngseok Kim and Choongik Kim *

Metal-oxide semiconductors are considered promising alternative materials in the field of flat panel display industry due to their advantages, such as high mobility, transparency, uniformity, low production cost, and large-area processability. Nevertheless, stress-induced instability in metal-oxide thin-film transistors should be addressed for further applications. Various external stresses, such as voltage, illumination, heat, and ionizing radiation, have been known to affect the defect states in metal-oxide thin-film transistors, resulting in degradation of electrical performance, such as threshold voltage, mobility, and subthreshold swing. Therefore, recent research efforts have been focused on the prevention/reduction of defect generation in oxide semiconductors and the adjustment of defect states in the sub-gap by various approaches, such as introducing novel materials, optimizing fabrication processes, and improving device structures. This highlight article provides an overview of recent research efforts to enhance the stability of metal-oxide thin-film transistors against various external stresses. External stresses are categorized into five different types and degradation mechanisms as well as approaches for the enhancement of device stability for each stress are discussed. This highlight article intends to inspire new studies on metal oxide thin-film transistors for developing state-of-the-art electronic devices.

Received 5th February 2023,
Accepted 7th May 2023

DOI: 10.1039/d3tc00417a

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1. Introduction

As technology in the display industry has improved to realize organic light-emitting diodes (OLEDs) with ultra-high definition and high frame rate, backplane thin-film transistors (TFTs) with high switching rates have been in great demand.[1–3] Metal oxide-based semiconductors as active layers of TFTs could fulfill these technological requirements and advance to the next generation of flat panel display technology.[4–7] In 2004, Nomura *et al.* developed the first practical oxide TFT channel material, amorphous indium–gallium–zinc oxide (a-IGZO), which exhibited high electrical performance.[8] Amorphous oxide semiconductors (AOSs) have been considered as an alternative to amorphous silicon (a-Si)

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due to their advantages, such as high field-effect mobility over 10 $cm^2 V^{-1} s^{-1}$ and optical transparency.[9–11] These AOSs also offer advantages in terms of uniformity, production cost, and processability in large area compared to low-temperature poly-Si (LTPS) materials.[12] As a result of these benefits, several corporations such as LG Electronics, Samsung, Hitachi, and AU Optronics Corporation have developed the prototype of AOS TFT-based active matrix organic light-emitting diode (AMOLED) since the a-IGZO was reported in 2004.[13,14] In 2012, the first commercial a-IGZO TFT-based displays were produced by Sharp Corporation.[15] Since then, various corporations have employed a-IGZO TFTs in ultra-high-definition (UHD) large-sized OLED TVs.[15]

In spite of these merits of AOSs, relatively low stability and reliability issues of the corresponding materials still remain to be addressed.[16,17] Various external stresses such as voltage, illumination, heat, and ionizing radiation have been known to degrade the electrical performance of AOSs.[18–21] The instability of AOS TFTs caused by these external stresses is related to the structural defects in the bulk semiconductor, the back-channel surface, which is the further region from the bulk semiconductor, the gate dielectric, and the front-channel region, which is near the semiconductor–dielectric interface (Fig. 1).[22] Structural defects, such as atomic vacancy, substitution, anti-site, interstitial atoms, and dangling bond, have been known to form the sub-gap states in the bandgap of AOSs.[20,23,24] These defect states can deteriorate the electrical performance parameters of AOS TFTs, such as mobility, threshold voltage (V_{th}), and subthreshold swing (SS).[16,25,26] For example, the formation of shallow donor states in the channel, positive charge trapping at the semiconductor–dielectric interface, and the gate dielectric can cause a negative shift in V_{th} and increase carrier mobility in AOS TFTs.[27] On the other hand, the formation of acceptor-like traps in the bulk semiconductor and negatively charged traps at the semiconductor–dielectric interface and the gate dielectric tend to induce positive V_{th} shift in the transfer curve and decrease carrier mobility of the devices.[28] In addition, this can also lead to a degradation of the SS parameter, which indicates the switching performance of TFTs in the near-V_{th} region due to the formation of defect states caused by external stresses.[29] The SS increases with the interface trap density of AOS TFTs, indicating lower switching performance.[30] For instance, electron trapping in the bulk channel or semiconductor–dielectric interface during positive bias stress (PBS) has been known to deteriorate the SS value.[31] Although various electrical parameters change due to external stresses, the shift of the V_{th} value is one of the most important parameters for determining the stress stability of AOS TFTs.[32] Several groups have reported that V_{th} shifts more dramatically under external stresses with little change in SS and mobility values.[33–35] Furthermore, the shift in V_{th} value would result in abnormal turn-off or turn-on in the display pixel circuit.[32] Therefore, V_{th} stability can be considered the most critical property of the AOS TFTs.[32]

The TFT devices should be able to tolerate external stresses and perform consistently for a long period of time.[36] Device instability originating from stress-induced defects can be improved in various ways. For instance, the deposition of a passivation layer on the back-channel of AOS could be one of the simple methods to improve the stability of AOS TFTs.[37] The role of the passivation layer is to shield the active layer from external impurities such as H_2O and O_2 molecules in the ambient environment.[38] Specifically, the adsorption of O_2 molecules onto the AOS surface can provide acceptor-like states at the back-channel region.[39] Similarly, H_2O molecules on the metal-oxide surface can act as a donor-like surface state.[40] In addition to blocking external ambient species, the passivation layer could also fill up the defects in AOSs, such as vacancies and dangling bonds, resulting in the reduction of acceptor-like and donor-like traps, alleviating external stresses upon AOS TFTs.[41,42] Doping metal cations, which act as oxygen binders, could also be another way to improve the stability of AOS TFTs *via* the reduction of structural defects.[43] Oxygen vacancy defects, which are one of the main causes of degradation in the AOSs, should be controlled to be insensitive to external stresses.[44,45] Metal cations such as In and Zn form relatively weak chemical bonding with oxygen anion and tend to generate oxygen vacancies easily.[46] Thus, dopants with high metal–oxygen bond strength such as Y, W, Mg, and lanthanides can control the oxygen vacancy concentration in the AOS channel.[47–51] In addition to their characteristic of high bonding strength with oxygen, metal cations doped into oxide semiconductors can also affect the energy band gap configuration of AOSs. Hence, controlling the band gap of AOSs by doping metal cations would be an effective approach to achieving stability of the corresponding compounds.[52] For instance, increasing the band gap of AOS by doping can suppress the generation of electron–hole pairs induced by illumination or thermal stresses.

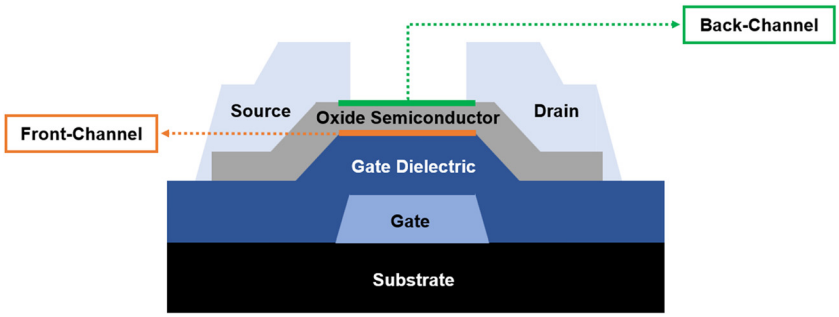

Fig. 1 The schematic diagram of the cross-sectional view of bottom-gate and top-contact metal-oxide thin-film transistor structure.

Furthermore, recently, it has been reported that doping certain metal cations can suppress the activation of V_O.[53] Specifically, doping certain metal cations such as tetravalent lanthanides can prevent the activation of V_O under illumination stress by converting incoming illumination to non-radiative transition due to charge transfer transition.[54] Thus, choosing an appropriate amount of dopants can result in AOS TFTs with high stability.[52,55] In addition to the methods mentioned above, research on the various ways to suppress the defects vulnerable to stresses has been widely investigated (*vide infra*).[56,57]

To this end, in this highlight, we investigate the stability issues of AOS TFTs under various external stresses and provide an overview of recently reported approaches to overcome each stress-related degradation of the devices. External stresses on AOSs are categorized into five different types: (i) voltage bias stress, (ii) illumination stress, (iii) heat stress, (iv) illumination and heat stress, and (v) ionizing radiation stress. The degradation mechanism of AOS TFTs under each type of stress will be explained. Then, we summarize some of the recent representative approaches to overcome the external stress-induced instability of AOSs, mostly in terms of reducing the V_{th} shift. Finally, we emphasize the importance of achieving device stability of AOS TFTs in the conclusion and outlook. Therefore, this highlight intends to expand the use of AOSs and encourage further investigation into the development of stable, high-performance optoelectronics.

2. Stress induced by voltage bias

The stability of AOSs is mainly affected by voltage bias stress due to intrinsic structural defects in bulk semiconductors, such as ion vacancies, substitutions, and dangling bonds.[45,58,59] For instance, when positive bias stress (PBS) is applied at the gate electrode of AOS TFTs for a period of time, the transfer curve shifts to a positive direction, and the drain current decreases continuously due to negatively charged traps.[31,35] Electrons are captured at the trap states of the channel and semiconductor–dielectric interface, and those are injected into the gate dielectric layer.[31,35] Consequently, negative localized trapped charges at the semiconductor and dielectric require a larger gate voltage to flow appropriate drain current (Fig. 2(a)).[60] On the other hand, positively charged donor states would be easily generated by negative gate bias because the formation energies of ionized oxygen vacancy (V_O^{2+}) would be lowered.[61] During negative bias stress (NBS), the V_O^{2+}s would migrate to the semiconductor–dielectric interface and become the positively charged traps.[61,62] Therefore, these would induce additional electrons and a negative shift in the threshold voltage values (Fig. 2(b)).[62] In addition to the degradation mechanisms related to charge trapping that have been previously demonstrated, it has been reported that abnormal phenomena can occur during gate bias stress due to other causes. For example, the residual mobile ions present in the channel/dielectric interface or dielectric layer can induce counterclockwise hysteresis during PBS tests due to the formation of an electron double layer (EDL) at the channel/dielectric interface, which induces undesired capacitance.[63] Furthermore, gas adsorption on the surfaces of oxide semiconductor films by OH species can increase the number of electrons through electrochemical reactions that generate free electrons in the AOS layer.[64] Thus, PBS test under high humidity conditions may result in a negative V_{th} shift due to the electron donation effect of H_2O molecules.[65] In addition, slow polarization in the gate dielectric including polar groups could affect the counterclockwise hysteresis under bias stress.[66,67] In other words, device instability under gate bias stress can be affected by various causes.

In addition to the gate bias stress effect on AOS TFTs such as PBS and NBS, as described above, drain bias stress has also

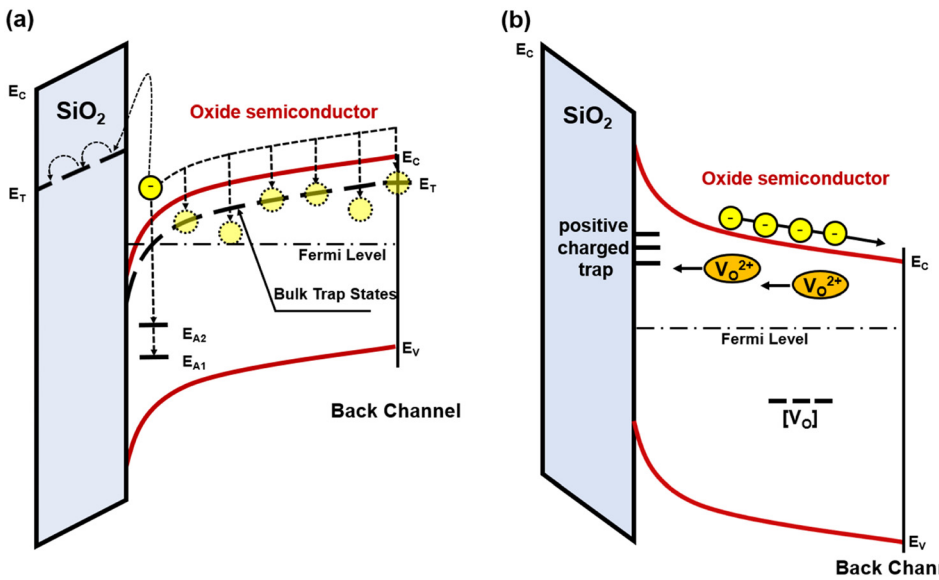

Fig. 2 Schematic of degradation mechanism of AOS under (a) positive bias stress (PBS) and (b) negative bias stress (NBS). Copyright 2020 The Royal Society of Chemistry. Reproduced with permission from ref. 37.

Table 1 Threshold voltage shift and methods to enhance the stability of metal-oxide thin-film transistor under bias stress

		Stress					
Year	Channel	Type	Time (s)	Applied voltage (V)	Method	ΔV_{th}[a] (V)	Ref.
2014	IGZO	PBS[b]	10 000	20		12.0	79
	IGZO	PBS	10 000	20	Vertircally graded V_O[d]	5.6	
2014	IZO	PBS	3600	20		3.4	81
		NBS[c]	3600	−20		−0.1	
	IZO:Al	PBS	3600	20	Doping Al	1.7	
		NBS	3600	−20		−1.4	
	IZO:Ga	PBS	3600	20	Doping Ga	1.6	
		NBS	3600	−20		−1.0	
	IZO/IZO:Al	PBS	3600	20	Bilayer structure	1.3	
		NBS	3600	−20		−0.32	
	IZO/IZO:Ga	PBS	3600	20		1.1	
		NBS	3600	−20		−0.2	
2016	IGZO	PBS	3000	5	Gate-insulator deposition (PEALD[e])	0.82	84
	IGZO	PBS	3000	5	Gate-insulator deposition (THALD[f])	0	
2017	IGZO	PBS	3600	50		−18.96	86
	IGZO	PBS	3600	50	PCBM[g] passivation	1.36	
2021	ITZO	NBS	3600	−20	No annealing after PR[h] contamination	−11	89
	ITZO	NBS	3600	−20	Annealing after PR contamination (300 °C)		
	ITZO	NBS	3600	−20	Annealing after PR contamination (350 °C)		
	ITZO	NBS	3600	−20	Annealing after PR contamination (400 °C)	−0.02	

[a] Threshold voltage shift (ΔV_{th}) during stress. [b] Positive gate bias stress. [c] Negative gate bias stress. [d] Oxygen vacancy. [e] Plasma-enhanced atomic layer deposition. [f] Thermal atomic layer deposition. [g] [6,6]-phenyl-C61-butyric acid methyl ester. [h] Photoresist.

been known to affect device stability.[68,69] The lateral electric field formed under a drain bias stress accelerates the electrons in the AOS channel, and the accelerated electrons collide with the neutral oxygen vacancies and ionize them.[70,71] The energy levels of ionized oxygen vacancies induced by drain bias are located near the conduction-band minimum (CBM).[71] The positively ionized defects accumulate additional electrons due to the conservation of charge neutrality, resulting in the degradation of the device performance.[71] However, there were several exceptional reports indicating that applying a large drain bias could suppress degradation under negative gate bias and illumination stress (NBIS), contrary to previous explanations.[72,73] A large negative drain voltage bias can induce the formation of an electric field towards the drain electrode on the drain side of a TFT. As a result, this could lead to the accumulation of ionized oxygen vacancies in the drain region during NBIS.[72] Subsequently, it can easily neutralize the positively charged oxygen vacancies by recombination with electrons injected from the drain electrode, thereby suppressing donor-like states.[72] Furthermore, AOS TFTs can be degraded by alternative current (AC) bias stress as well as direct current (DC) bias stress. The AC bias stress inevitably deteriorates the electrical performance of AOS TFTs under practical operations of the display pixel array.[74,75] The main cause of AOS TFTs under AC stress has been known to be hot carrier effects (HCEs) induced by accelerated carriers with high kinetic energies.[76] Under pulsed bias stress, the carriers in the AOS channel collide with the metal oxide lattice and break the weak atomic bonds.[77] This affords the generation of defect states, which capture electrons,[78] resulting in drain current degradation and generation of hump-like behavior in the transfer characteristic of TFTs.[77] Although it is of utmost importance to come up with a solution to solve the degradation of AOS TFTs under drain bias and AC stress, research on improving device instabilities from both stresses has rarely been conducted, compared to research on gate bias stress. Therefore, the approaches to improve the instabilities induced by gate bias stress will be mainly introduced in this section.

To this end, there have been recent efforts to investigate the mechanism of defect state generation under gate bias stress and find solutions to prevent or overcome the degradation of the electrical behavior of AOS TFTs (Table 1). First, oxygen vacancy (V_O) usually acts as electron trap states, affording poor PBS stability of AOSs.[20] Thus, controlling the concentration of V_Os in the channel layer *via* various methodologies could be an approach to enhance the stability of AOS TFTs. For instance, Park *et al.* fabricated a-IGZO that has the front channel with high oxygen vacancy concentration and a back channel with low oxygen vacancy concentration, which resulted in an improvement of PBS stability of the resulting TFTs (Fig. 3(a)).[79] The a-IGZO semiconductor layers were formed by radio frequency (RF) magnetron sputtering method with different times for the 0% and 5% oxygen partial pressure, with the time ratios of 0% and 5% oxygen partial pressures of 100 : 0 and 25 : 75, to fabricate these devices with controlled oxygen vacancy concentration. These samples were termed L100 TFT and H25/L75 TFT, respectively. In this report, a PBS test with 20 V was performed on both devices for 10 000 s, resulting in a V_{th} shift of 5.6 V and 12.0 V for H25/L75 and L100 TFT, respectively (Fig. 3(b) and (c)). These results show that the PBS stability of H25/L75 TFT with the reduced V_O concentration at the back-channel, compared to that of the L100 TFT, was improved by a factor of greater than 2 in terms of V_{th} shift. Since one of the main causes of PBS instability in AOS TFTs is the interaction between the back-channel and ambient environments, the low V_O concentration in the back channel could act as the self-

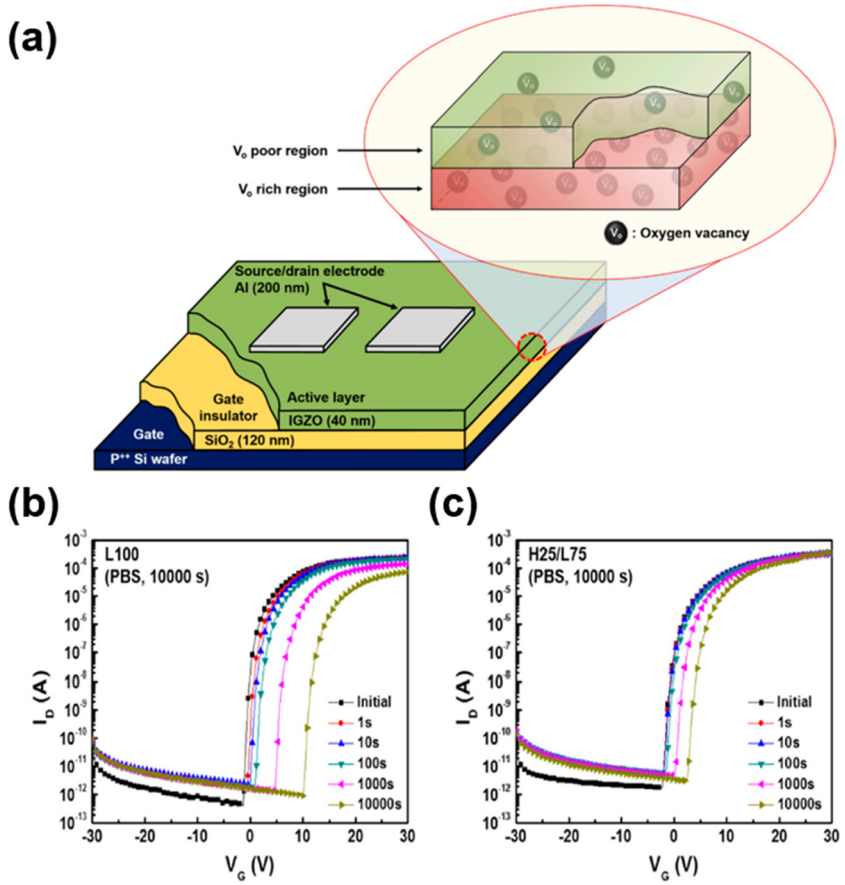

Fig. 3 (a) Schematic diagram of TFT with vertically graded oxygen vacancy active layer, PBS test results of a-IGZO TFTs with (b) L100 and (c) H25/L75. Copyright 2014 American Chemical Society. Reproduced with permission from ref. 79 (time ratios of 0% and 5% oxygen partial pressures during the fabrication of IGZO active layers of 100 : 0 and 25 : 75 are termed L100 and H25/L75, respectively).

passivation layer of a-IGZO, which decreases the back-channel exposure to the ambient environment.[80]

Seo *et al.* similarly tried to control the oxygen vacancy concentration in AOSs and investigated the effects of aluminum or gallium doping in In–Zn–O (IZO:Al or IZO:Ga) on the bias stability of TFTs (Fig. 4(a)).[81] Al and Ga are known to be effective oxygen vacancy suppressors as they strongly bind oxygen anions due to their high ionic potential.[6] When the oxygen vacancy suppressors, such as Al and Ga, were doped into IZO, the on-current and mobility of TFTs decreased with increasing concentrations of Al and Ga doping. Although doping with Al and Ga suppressed oxygen vacancy generation, the single-layer IZO:Al and IZO:Ga TFTs showed threshold voltage shifts of −1.4 V, −1.0 V under −20 V NBS, and +1.7 V and +1.6 V under 20 V PBS for 3600 s, respectively. Meanwhile, the single-layer IZO TFT showed high NBS stability with a V_{th} shift of −0.1 V, but poor PBS stability with V_{th} of +3.4 V. Interestingly, the introduction of dopants only improved the PBS stability but deteriorated the NBS stability of the single-layer structure. Authors further employed the bilayer structure TFT to improve the PBS stability compared to single-layer TFT *via* the reduction of trap sites by thermal diffusion of back-channel composition.[82,83] The resulting bilayer TFT structure comprising IZO (bottom layer) and IZO:Ga (top layer; 4 mol%) performed stably under bias stresses with V_{th} shifts of −0.2 V under NBS and +1.1 V under PBS, respectively (Fig. 4(b)).

The TFTs with top-gate structures are usually applied in ultra-high definition displays due to their low RC delay. Therefore, the relation between the degree of PBS stability and the gate insulator deposition methods in top-gate/bottom-contact TFTs was investigated by Kim *et al.*[84] Different types of deposition methods, such as thermal atomic layer deposition (THALD) and plasma-enhanced ALD (PEALD), were employed for the first gate insulator (Al_2O_3) to study the effect of the deposition process on the a-IGZO channel. The different types of TFTs whose first gate insulator was deposited by THALD and PEALD were named samples A and B, respectively (Fig. 5(a)). As shown in Fig. 5(b) and (c), the subthreshold swing (SS) characteristic of sample A was superior to that of sample B due to the lower interface trap density value of sample A. Specifically, the PEALD process on the a-IGZO layer surface led to increased trap density near the semiconductor–insulator interface due to the damage caused by oxygen plasma on the a-IGZO surface.[85] Hence, sample B showed a positive shift (up to 0.82 V) in threshold voltage during a stress time of 3000 s due to the trapping of electrons at the interface and bulk oxide,

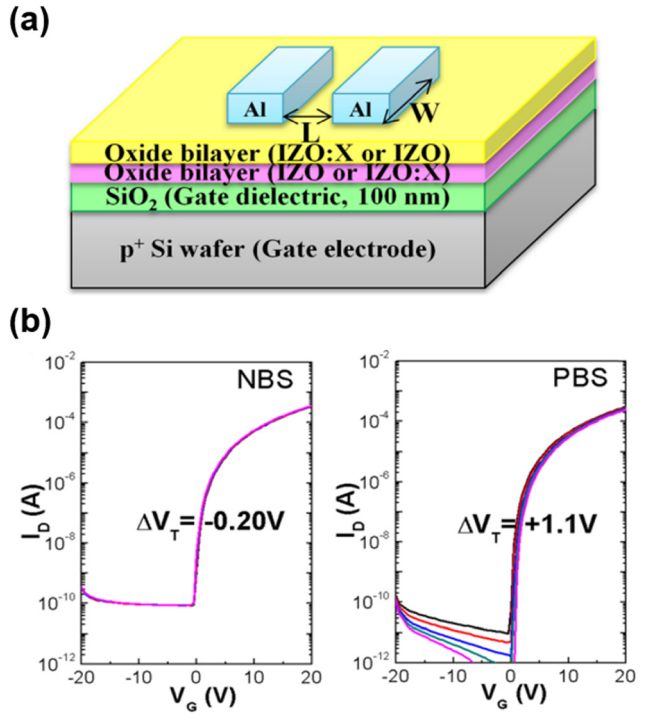

Fig. 4 (a) Structure image of oxide TFT, (b) negative (−20 V) and positive (+20 V) gate bias stability of active bilayer IZO/IZO:Ga TFTs (V_{DS} = 20 V, V_G = −20 to +20 V). Copyright 2014 American Chemical Society. Reproduced with permission from ref. 81.

while sample A showed a ΔV_{th} value of ~0 V under PBS test (Fig. 5(b)–(d)).

Since the defect states of the back channel of AOSs significantly affect the TFT performance and stability, the passivation of the back channel with appropriate materials could be a solution to enhance the stability of AOS TFTs.[37] In 2017, our group investigated the multifunctional organic passivation layer between a-IGZO and copper electrode to prevent copper ion migration and ensure high bias stability of the TFTs (Fig. 6(a)).[86] Copper ion migration to the a-IGZO layer can generate acceptor- or donor-like traps and induce device instability.[87] According to the hard–soft acid–base (HSAB) theory, copper ions, which are regarded as soft acids, chemically interact with organic semiconductors composed of S and P atoms and delocalized π-electrons, which are regarded as soft bases. Thus,[6,6]-phenyl-C61-butyric acid methyl ester (PCBM) layer on a-IGZO could effectively block copper-ion diffusion, resulting in a small V_{th} shift of 1.36 V under PBS conditions (V_{DS} = 25 V, V_G = 50 V) for 3600 s (Fig. 6(b)). In addition to blocking copper-ion migration, the PCBM layer could also act as a passivation layer suppressing the effect of external impurities such as H_2O and O_2 on the a-IGZO layer.[88]

Recently, Shiah *et al.* reported the mechanisms of instabilities in AOSs induced by carbon monoxide (CO)-related impurities during the photolithography process and improved the stability of amorphous In–Sn–Zn–O (a-ITZO) TFTs through

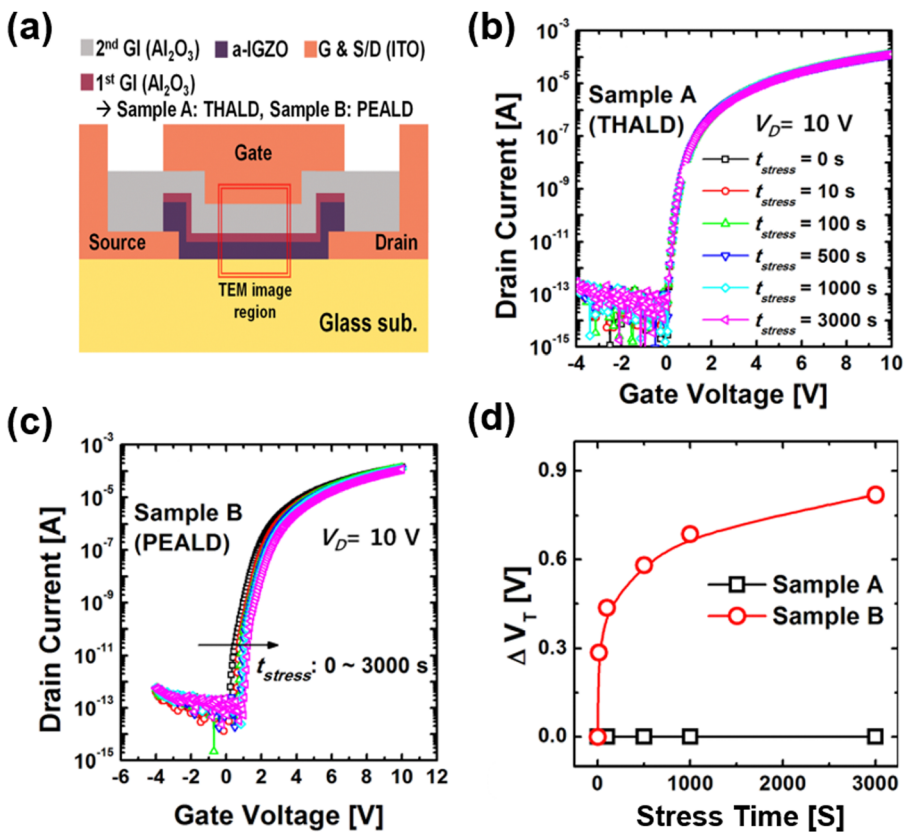

Fig. 5 (a) Device schematic of the TFTs, Transfer curves during the PBS test of (b) sample A and (c) sample B, (d) comparison of the variation of V_{th} *versus* the stress time, with a V_G value of 5 V applied for 3000 s during the PBS test. Copyright 2016 American Institute of Physics. Reproduced with permission from ref. 84.

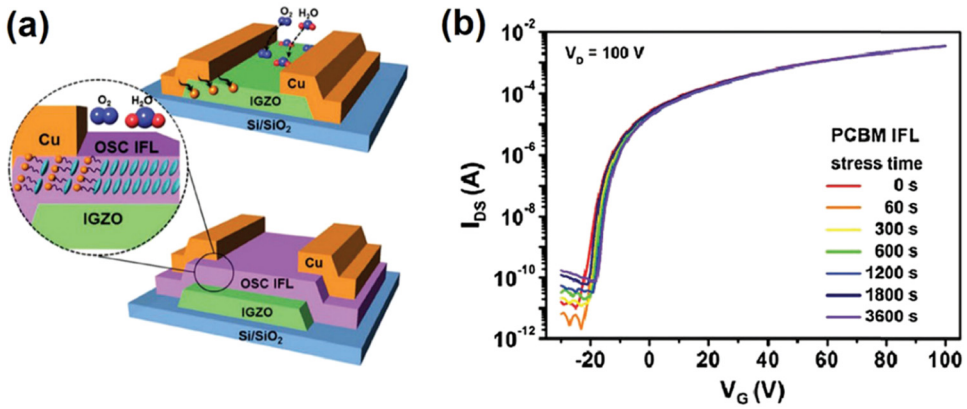

Fig. 6 (a) Schematics showing the device structures of a-IGZO TFTs with and without organic semiconductor interfacial layers, (b) a-IGZO TFTs with PCBM interlayer with respect to the stress time under a drain bias of 100 V. Copyright 2017 Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim. Reproduced with permission from.[86]

post-deposition annealing.[89] A large number of CO-related impurities in AOS could occur during the photolithography process due to the chemical reactions between oxide semiconductors and photoresist (PR). These CO-related impurities would act as donor-like states, causing a shift downwards in the Fermi level of AOS during NBS, and the adsorbates would donate free electrons to the CBM of AOS.[90] Thus, a severe negative shift in the transfer curve occurs due to CO-related impurities. To overcome the detrimental impurities, post-deposition annealing at high temperatures above 350 °C is required to improve the NBS stability (Fig. 7(a)–(d)). Therefore, the a-ITZO TFT without annealing after PR contamination exhibited a V_{th} shift value of −11 V, while the most stable a-ITZO with annealing at 400 °C exhibited a V_{th} shift value of −0.02 V under NBS.

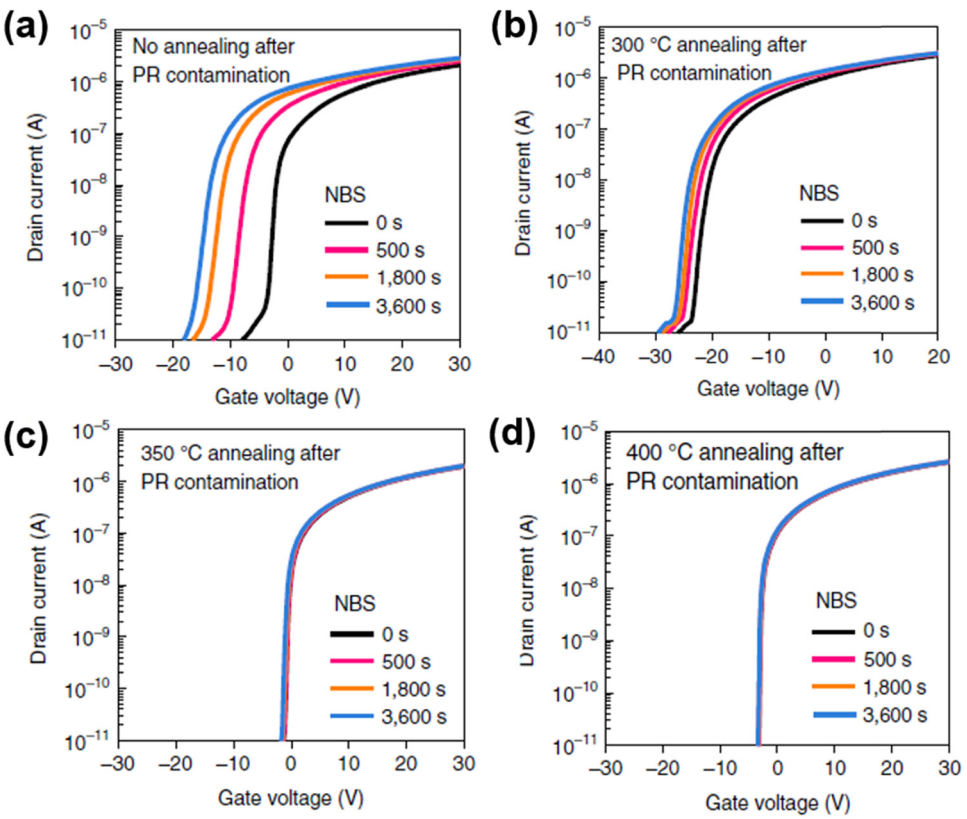

Fig. 7 NBS results of ITZO TFT samples (a) before annealing and (b) after annealing at 300 °C, (c) 350 °C, and (d) 400 °C. For the NBS test, a negative bias of V_G (−20 V) was applied. Transfer curves were taken with a drain–source voltage of 0.1 V. Copyright 2021 Springer Nature. Reproduced with permission from ref. 89.

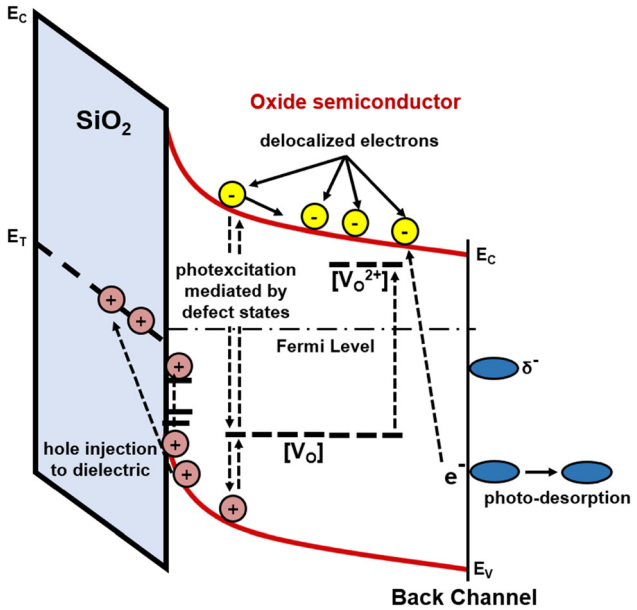

Fig. 8 The scheme of degradation mechanism of AOS under negative bias illumination stress (NBIS).

3. Stress induced by illumination

In addition to the effects of voltage bias stress on AOS TFTs, illumination can also cause the degradation of the device electrical performance.[91] In the display array, light exposure to AOS TFTs in the backplane is unavoidable due to the backlight units. Furthermore, for transparent electronic devices, AOSs would inevitably be exposed to external illumination. Under negative gate bias with light illumination, it is commonly known that the transfer curve shifts in the negative direction.[92] Light illumination induces the generation of electron–hole pairs mediated by the defect states and the photoexcitation of neutral oxygen vacancies defects (V_O) to form ionized oxygen vacancies (V_O^{2+}).[93,94] Negative gate bias would make photoexcited holes migrate toward the front channel.[94] During this process, the photo-created holes become trapped at the interfacial trap state and are subsequently injected into the gate dielectric layer. Furthermore, the transition of V_O states to V_O^{2+} shallow states induced by illumination would result in the generation of additional delocalized electrons in the CBM.[53] Especially in ambient atmosphere, light exposure would also lead to the oxygen desorption at the back-channel surface of AOS, resulting in the addition of free electrons in the channel.[95] Therefore, negative bias illumination stress (NBIS) reduced the threshold voltage values needed to achieve the same drain current and caused a negative shift in the threshold voltage values (Fig. 8).[92] To this end, various approaches have been investigated to overcome the stresses induced by illumination in AOS TFTs (Table 2). For instance, given the mechanism of the generation of ionized oxygen vacancy defects by light illumination, methods to suppress/prevent the formation of oxygen vacancies in the AOSs would be one approach to enhance the stability of the devices against illumination stress.

As described above, the passivation of the AOS back-channel layer can enhance the stability of AOS TFTs under illumination stress.[96] Yang *et al.* employed PEALD-derived AlOx as the passivation layer for the Al–Sn–Zn–In–O (AT-ZIO) semiconductor under light-illuminated negative bias stress conditions to prevent the interaction between the back-channel surface and ambient environment.[95] Fig. 9(a) shows that light exposure induces the desorption of the oxygen species adsorbed to the back-channel surface of AOS due to the lower binding energy between the back-channel and oxygen species than photon energy (>2 eV). Photodesorption of oxygen species would lead to the release of free electrons into the bulk semiconductors, causing V_{th} shifts in the TFT.[97] Hence, the un-passivated AT-ZIO-based TFT exhibited a huge V_{th} shift of 11.5 V after applying NBS with green light illumination for 10^4 s, as shown in Fig. 9(b). On the other hand, the AT-ZIO-based TFT device passivated with PEALD-derived AlO_X showed a much smaller shift of V_{th} value (0.72 V) under the same condition (Fig. 9(c)). Therefore, the light-induced bias stability of oxide TFTs could be improved using a suitable passivation layer.

Yun *et al.* introduced the multivalent V cation, which acts as an oxygen vacancy suppressing dopant, into the zinc-tin oxide (ZTO) channel and attempted to fabricate a bilayer TFT with both high stability and mobility.[98] Vanadium is considered a V_O suppressor in ZTO semiconductor materials due to its high Gibbs free energy for the formation of V_O and bond dissociation

Table 2 Threshold voltage shift and methods to enhance the stability of metal-oxide thin-film transistors under illumination stress

		Stress					
Year	Channel	Light source	Time (s)	Applied voltage (V)	Method	ΔV_{th}[a] (V)	Ref.
2010	AT-ZIO	530 nm, 0.1 mW cm^{-2}	10 000	−20		−11.5	95
	AT-ZIO	530 nm, 0.1 mW cm^{-2}	10 000	−20	Al_2O_3 passivation	0.72	
2015	ZTO	550 nm, 0.1 mW cm^{-2}	5000	−30		−7.3	98
	VZTO/ZTO	550 nm, 0.1 mW cm^{-2}	5000	−30	Bilayer structure	−0.9	
2018	IGZO	Halogen lamp	2000	−30			102
	IGZO	Halogen lamp	2000	−30	Cyclic annealing		
2018	IZO	White LED 12 000 cd m^{-2}	7200	−20		−16.5[b]	105
	PrIZO	White LED, 12 000 cd m^{-2}	7200	−20	Doping Pr	−2.0[b]	
2019	IZO	White LED, 11 000 lux	3600	−20		−11	107
	ZGO	White LED, 11 000 lux	3600	−20	Bandgap engineering	0	

[a] Threshold voltage shift (ΔV_{th}) during stress. [b] Turn-on voltage shift during stress.

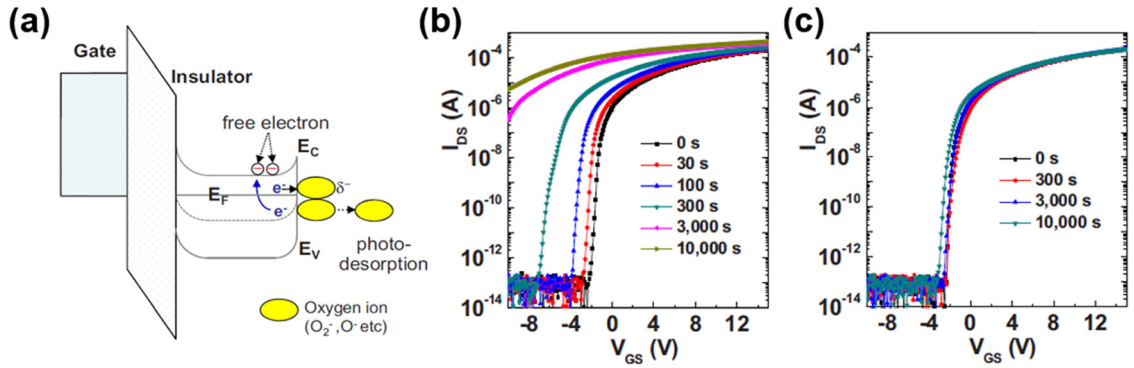

Fig. 9 (a) Schematic energy band diagram showing the photodesorption of oxygen molecules into the ambient atmosphere for the un-passivated device under the application of NBS. The desorption of oxygen ions would result in an increase in the net free carrier density, enhancing the negative V_{th} shift in oxide TFTs. (b) The evolution of the transfer curves for the unpassivated device and (c) passivated device with increasing NBS time upon green light irradiation. Copyright 2010 American Institute of Physics. Reproduced with permission from ref. 95.

energy between vanadium and oxygen. However, the vanadium-doped ZTO (VZTO) layer showed semi-insulating behavior in TFTs due to a significant reduction of Sn and V metal ions. Therefore, the authors employed a VZTO/ZTO bilayer as the active layer and compared the electrical characteristics of bilayer structure TFTs with those based on ZTO during stress testing. Under the NBIS test, the ZTO-based TFT exhibited severe changes in electrical characteristics. The ΔV_{th} values of ZTO TFT under illumination stress (IS) only and under NBIS for 5000 s were −2.1 V and −7.3 V, respectively (Fig. 10(a)). On the other hand, the transfer curve of VZTO/ZTO TFT changed slightly with a ΔV_{th} value of 0.9 V (Fig. 10(b)). In X-ray photoelectron spectroscopy (XPS) analysis, the relative peak area of V_O in the ZTO layer was 13.7%, and it reduced to 4.5% in the VZTO/ZTO layer. This indicates that the VZTO/ZTO bilayer TFT has fewer donor-like defects activated under 550 nm light illumination compared to ZTO-based single-layer TFT (Fig. 10(c) and (d)). Therefore, the VZTO/ZTO-based TFT ensured both high mobility and high stability under illumination stress compared to the VZTO single-layer TFT and ZTO single-layer TFT.

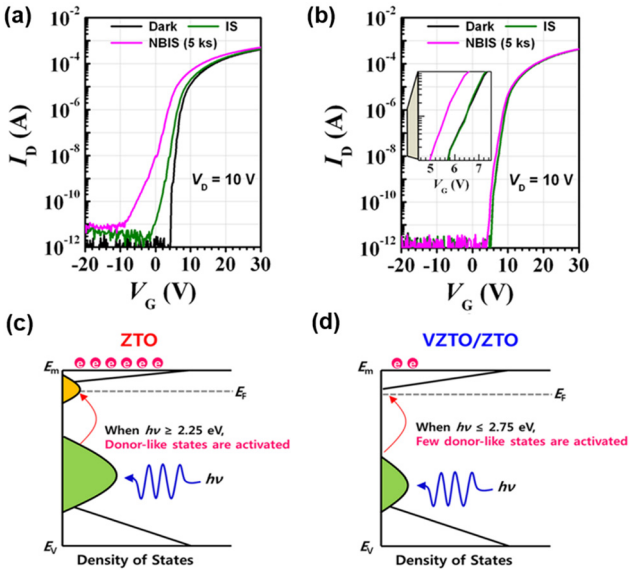

Fig. 10 Change in transfer curves of the (a) ZTO TFT and VZTO/ZTO bilayer TFT under illumination stress (IS) only and negative bias illumination stress (NBIS), Schematic illustrations of the change in the subgap states of (c) ZTO and (d) VZTO/ZTO films under IS. Copyright 2015 American Chemistry Society. Reproduced with permission from ref. 98.

Annealing conditions could also have a huge impact on the defect states in the AOS layer, thus affecting the electrical stability under illumination. To this end, various annealing methods for AOS have been investigated, including UV irradiation, microwave energy, temperature modulation, and partial pressure gases.[99–101] Especially in the study by Chen *et al.*, a cyclical low-temperature annealing process was employed to alleviate the NBIS-induced instability of the a-IGZO TFT.[102] The cyclical annealing process in O_2 ambient condition at 220 °C is composed of an alternating heating process progressed at 220 °C for 3 min followed by 1 min cooling period (Fig. 11(a)). This repeated annealing and cooling process would reduce the defects and facilitate the bonding of atoms in AOS. Metal–oxygen bonding is associated with atomic bond length. While a longer distance between metal and oxygen atoms makes it difficult to form bonds but conversely, closer metal/oxygen atoms tend to form stronger bonds (Fig. 11(b)).[103,104] In this experiment, oxygen vacancies in oxide semiconductors could effectively be filled by the cyclical annealing process, with an atom–oxygen bonding mechanism occurring during the repeated cooling phases. Therefore, a denser and stronger oxygen bond could be formed by the cyclical annealing method compared to the conventional long annealing process. A comparison between the cyclical annealing method and the conventional long annealing method is shown in Fig. 10(c) and (d). As shown, while the conventional an-hour annealing process afforded an improvement of V_{th} shift by 7.36 V (Fig. 11(c)), the cyclical annealing method resulted in a 13 V improvement in V_{th} value (Fig. 11(d)).

In 2019, Xu *et al.* investigated the effect of introducing praseodymium (Pr) ions into In–Zn–O (IZO) since moderate acceptor-like trap states formed by Pr ions would suppress photo-induced electrons in the conduction band and afford stable TFTs under illumination stress.[105] Normally, it is known

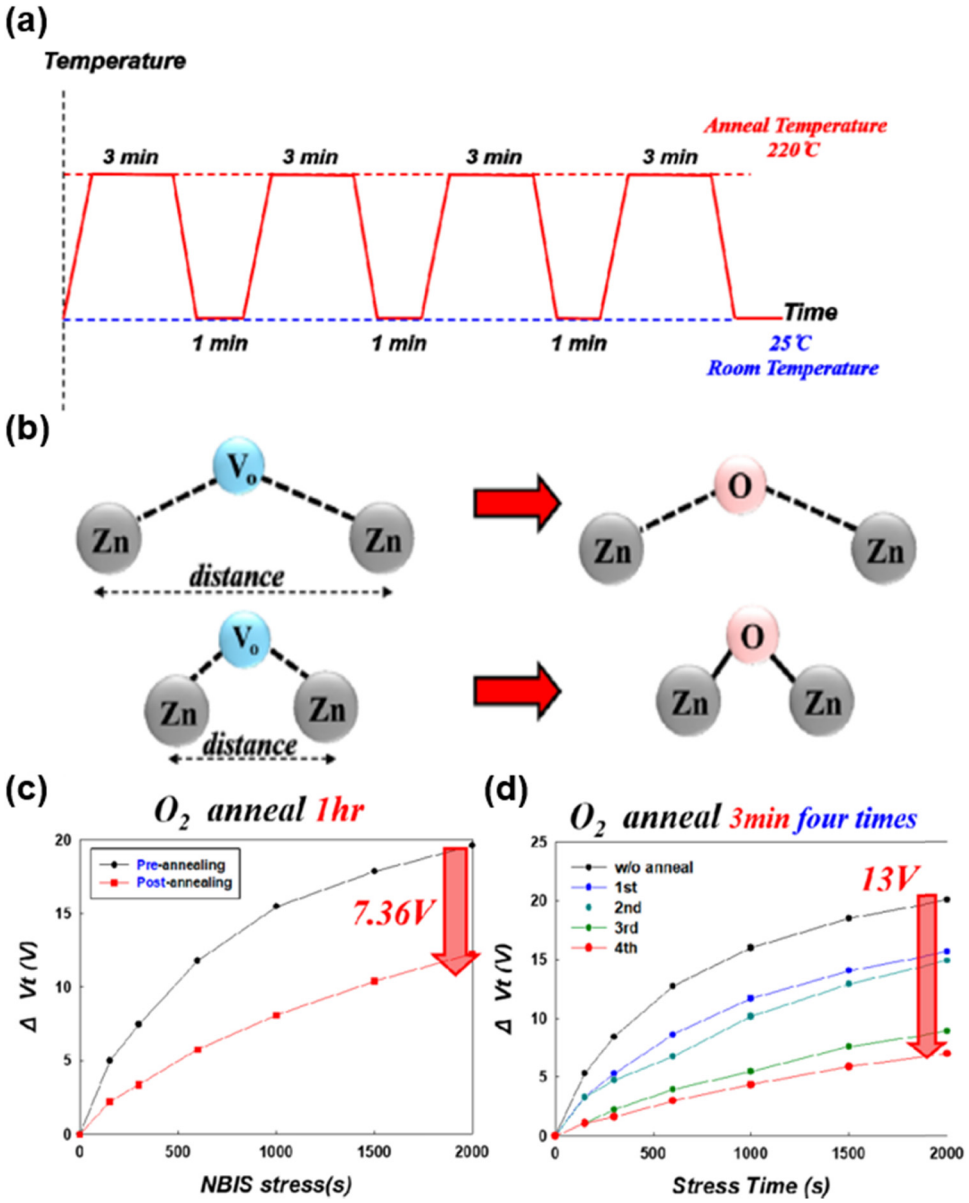

Fig. 11 (a) Steps of the cyclical annealing process, (b) if the atomic spacing is too far, it is not conducive to oxygen bonding, while the shorter atomic spacing favors oxygen bonding, (c) after uncycled oxygen annealing for 1 h, the V_{th} shift improves by 7.36 V, (d) after cyclical annealing, the V_{th} shift improves by 13 V. Copyright 2018 American Chemical Society. Reproduced with permission from ref. 102.

that V_O states near the valence-band maximum (VBM) would be excited to V_O^{2+} states that donate the delocalized electron to CBM.[27,106] Furthermore, with the doping of Pr, shallow acceptor-like trap states at ~0.3 V below CBM could be induced. Under illumination, photo-induced electrons are trapped by these acceptor-like trap states, resulting in the suppression of additional free carriers. Furthermore, the shallow acceptor-like states (Pr_H^+) charging with the photo-induced electrons would lower the energy of Pr_H^+ states (Pr_L^+) close to V_O states. This process would lead to the recombination of V_O^{2+} and the photo-induced electron to V_O and Pr_L^+ would recover to the initial Pr_H^+ states by relaxation. The Pr-induced traps would act as recombination centers for the photo-induced electrons and V_O^{2+} (Fig. 12(a)). Furthermore, doping of Pr in IZO leads to a decrease in the V_O ratio due to the strong bonding strength of Pr–O (753 kJ mol^{-1}), suppressing the V_O formation, as analyzed by XPS (Fig. 12(b)). Fig. 12(c) shows the transfer curves of PrIZO semiconductor under an NBIS without (0%) and with (2.98%) Pr doping, respectively. As shown, a V_{on} shift of −16.5 V with severe degradation of SS was observed for TFT without Pr doping, whereas the TFT with Pr doping (2.98%) exhibited a V_{on} shift of −2.0 V.

The sub-gap states of oxide semiconductors near the VBM could be one of the causes of photo-induced instability in AOS TFTs. Therefore, the energy difference between the sub-gap states and the CBM should be widened to be transparent over

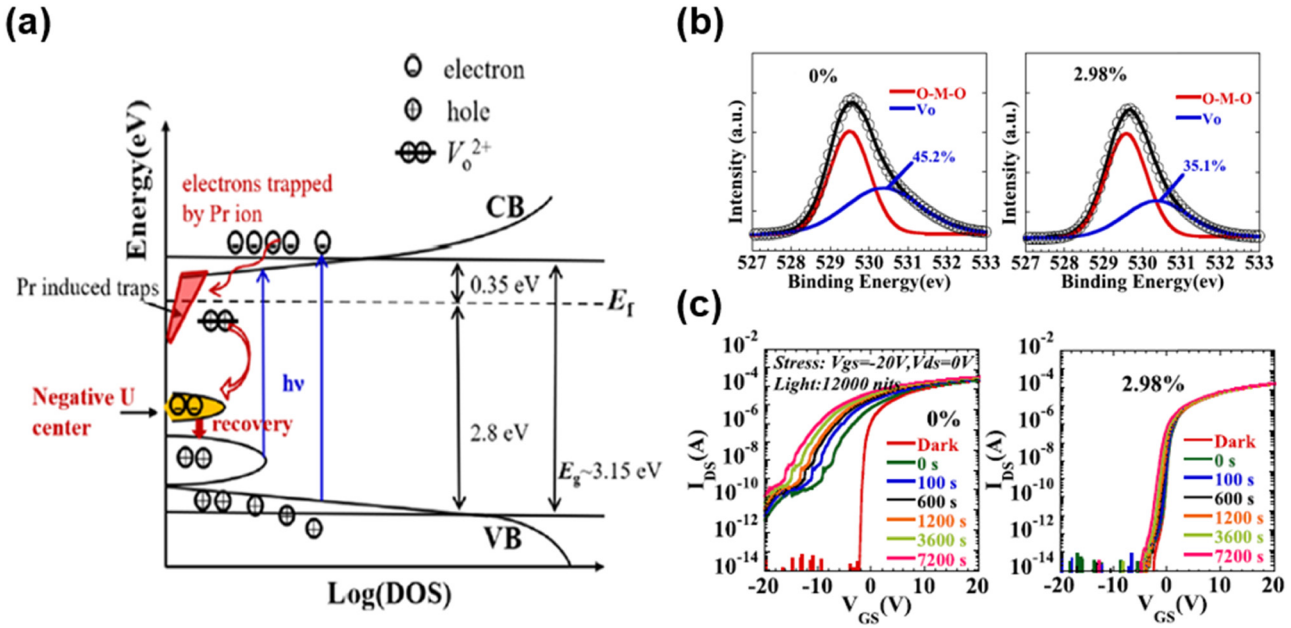

Fig. 12 (a) Sub-gap trap states model in Pr-doped PrIZO-TFTs, (b) XPS O 1s spectra of the 0 and 2.98% PrIZO thin films, (c) NBIS test for TFTs without (left) and with Pr doping (right). Copyright 2019 American Chemical Society. Reproduced with permission from ref. 105.

the entire visible-light region, in order to prevent light-induced instability of AOS TFTs. To this end, Kim *et al.* investigated the effect of widening the band gap (E_g) on the photo-stability of AOSs while retaining their electrical performance.[107] To widen the E_g, light metal cations such as Al and Si can be introduced, but this leads to small band dispersion, which could interrupt the electrical performance.[108] Thus, a wide E_g with high mobility can be attained by deepening the VBM and retaining the large conduction band dispersion (Fig. 13(a)). It was found that amorphous Zn–Ga–O (a-ZGO) showed a large variation in the energy level of VBM, corresponding to ionization potential, while the energy level of CBM remained unchanged. Covalent bond interaction between Zn 3d-orbital and O 2p-orbital makes the anti-bonding level shallow, whereas a-GaO_X has a deep ionization potential of 8.2 eV.[107] In other words, controlling the ratio of Zn/Ga would exhibit the appropriate energy level of the VBM (Fig. 13(b)). Consequently, the TFT with a-$Zn_{0.3}Ga_{0.7}O$, with the energy difference between the sub-gap states and the CBM of a-ZGO that is larger than ~3.0 eV, exhibited excellent photo-stability compared to a-IGZO and a-IZO, with little V_{th} shift. Furthermore, the field-effect mobility in the saturation regime of the a-ZGO TFT was ~9 $cm^2 V^{-1} s^{-1}$, which implies no degradation of electrical performance (Fig. 13(c)).

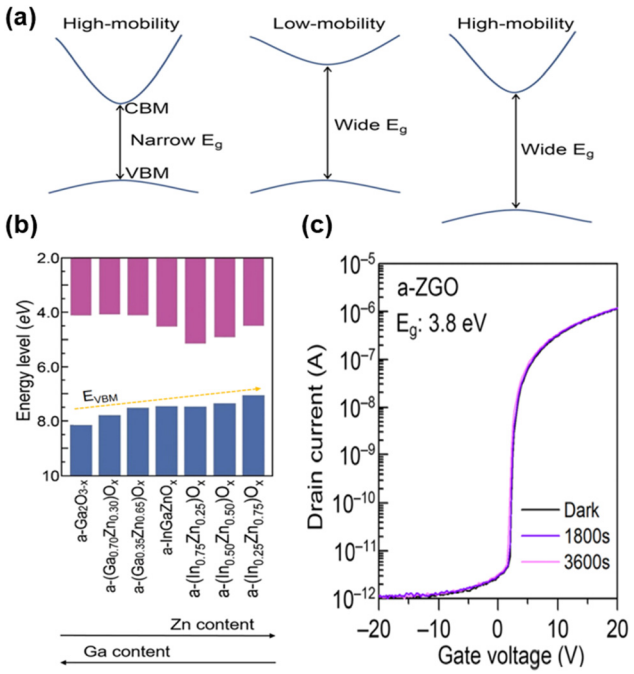

Fig. 13 (a) The expected electronic structures and electrical properties of conventional AOSs with (left) high electron mobility and a narrow E_g, (middle) low electron mobility and a wide E_g, (right) a proposed electronic structure with suitable photo-stability and high mobility. (b) Energy levels of various AOSs determined by *in situ* UPS, which are arranged in order of valence band maximum (VBM) level, (c) NBIS test results for TFTs fabricated from $Zn_{0.3}Ga_{0.7}O_x$ (E_g = 3.8 eV). Copyright 2019 American Institute of Physics. Reproduced with permission from ref. 107.

4. Stress induced by heat

Similar to bias and illumination stress, high temperature has also been known to degrade the electrical performance of AOS TFTs.[109] When the display pixel arrays operate for a long period of time, the heat generated by resistance in the circuits tends to induce thermal stress in AOS TFTs. When thermal stress is applied to AOSs, the electrons in the oxide semiconductors will be accelerated, resulting in high kinetic energy.[110] Highly energetic electrons would collide with both metal cations and

Table 3 Threshold voltage shift and methods to enhance the stability of metal-oxide thin-film transistors under heat stress

		Stress					
Year	Channel	Temperature (°C)	Time (s)	Applied voltage (V)	Method	ΔV_{th}[a] (V)	Ref.
2011	ZnO	60	7200	−20		−4.91	112
	Y–ZnO	60	7200	−20	Doping Y	−1.72	
2013	IGZO	60	3600	−20		−3.21	113
	IGZO:N	60	3600	−20	Doping nitrogen	−1.13	
2014	IGZO	100	10 000	20	SiO_X passivation	−6.24	114
	IGZO	100	10 000	20	SiN_X:F[c] passivation	−0.45	
2018	IZO	60	7200	20		9.52	115
	PrIZO	60	7200	20	Doping Pr	1.97	
2021	IGZO	50	10 000	20		9.22	116
	OSL[b]/IGZO	50	10 000	20	Oxygen scavenger layer	2.31	

[a] Threshold voltage shift (ΔV_{th}) during stress. [b] Oxygen scavenger layer. [c] Fluorinated silicon nitride.

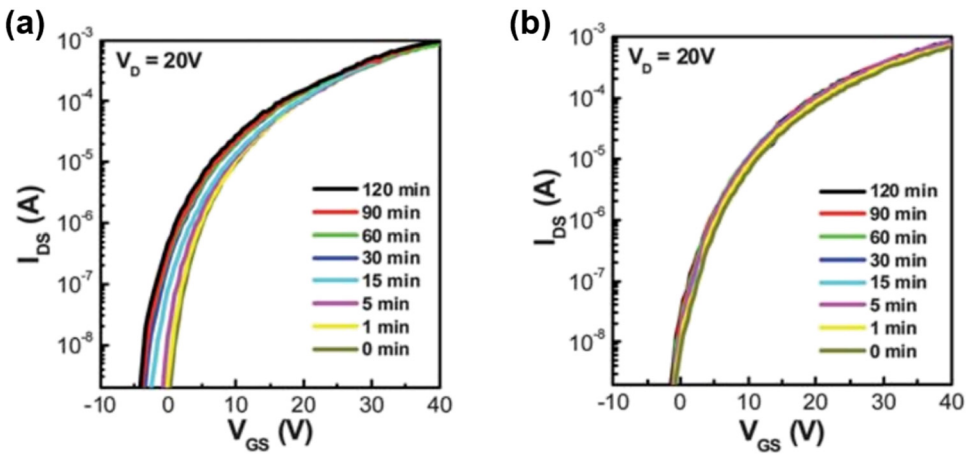

Fig. 14 (a) Variations in the transfer characteristics of TFTs fabricated with (a) ZnO and (b) 1% Y–ZnO under the NBTS condition of V_{DS} = 10 V, V_{GS} = −20 V, and T = 60 °C for a duration of 2 h. Copyright 2011 The Royal Society of Chemistry. Reproduced with permission from ref. 112.

oxygen anions, breaking the chemical bonds and generating interstitial and vacancy defects. Therefore, heat stress can cause a severe hump phenomenon and a shift in the threshold voltage in the transfer characteristics of AOS TFTs.[111] To prevent thermal stresses, various approaches have been carried out, such as doping in the AOS and introducing a passivation layer and an oxygen scavenger layer, as described below (Table 3).[112–116]

To overcome device instability caused by heat stress, Jun *et al.* employed yttrium (Y) as a dopant for the fabrication of solution-processed ZnO TFTs.[112] Since yttrium exhibits high oxygen-bonding energy (~719.6 kJ mol^{-1}), Y-doped ZnO-based TFT could efficiently reduce the oxygen vacancy and carrier concentration compared to pristine ZnO TFT. Thermal stress on AOSs would induce the excitation of electron–hole pairs, resulting in free electron carriers and trapped holes at interface trap states. As a result, these would cause a negative shift in threshold voltage values. In this study, the optimized TFT based on 1% Y-doped ZnO exhibited higher stability under negative-bias temperature stress (NBTS) test at 60 °C for 2 h with a ΔV_{th} of −1.72 V, compared to the ZnO-based TFT (ΔV_{th} of −4.91 V) (Fig. 14(a) and (b)). Apparently, broadening the optical band gap by doping with metallic cation (Y) having high bonding energy with oxygen resulted in the endurance of the devices against thermal stress due to the suppression of carrier excitation.

Similarly, to reduce the defect states in the AOS channel layer and interface, the effect of nitrogen (N) doping in a-IGZO

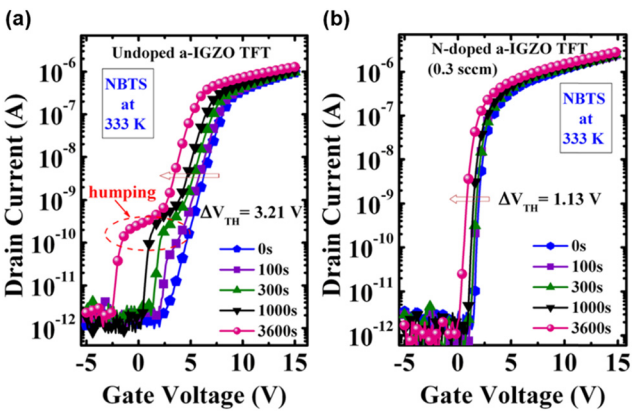

Fig. 15 NBTS stability of transfer curves of 20 V gate bias stressing at 333 K: (a) undoped and (b) N-doped a-IGZO devices. Copyright 2013 American Institute of Physics. Reproduced with permission from ref. 113.

on the stability of resulting TFT under NBTS was investigated by Raja *et al.*[113] Since the ionic radius of nitrogen is similar to that of oxygen, nitrogen could be an excellent substitution dopant for oxygen.[117] Hence, nitrogen atoms could compensate for the acceptor states and passivate intrinsic donor states in AOS films. As shown in Fig. 15, the N-doped a-IGZO TFT exhibited highly stable operation and high switching behavior in the subthreshold region, with field-effect mobility of 8.85 $cm^2\ V^{-1}\ s^{-1}$ and a low SS of 0.28 V dec^{-1}, compared to the undoped a-IGZO TFT (mobility of 9.82 $cm^2\ V^{-1}\ s^{-1}$ and SS of 1.10 V dec^{-1}). Especially, under NBTS test at 333 K for a duration of 3600 s, the N-doped a-IGZO device showed a smaller ΔV_{th} of 1.13 V than the undoped a-IGZO device (ΔV_{th} = 3.21 V) (Fig. 15).

In terms of trap passivation in AOSs, fluorine (F) is a promising candidate for passivating oxygen vacancies and weak bonds in oxide semiconductors. This is because its ionic radius is similar to that of an oxygen ion. During device operation, fluorine ions can fill in the weakly bonded oxygen and oxygen-deficient sites. Furthermore, the Zn–F bond strength (364 kJ mol^{-1}) is relatively high, and thus F could substitute weakly bonded Zn–O to form thermally stable Zn–F, providing stable device performance under thermal stress. Therefore, Jiang *et al.* studied the effect of a fluorinated silicon nitride (SiN_X:F) passivation layer on the PBTS stability of a-IGZO TFTs in comparison to a SiO_X passivation layer.[114] As shown in Fig. 16, a-IGZO TFTs with SiO_X passivation showed a negative V_{th} shift of −6.24 V with a hump behavior under PBTS

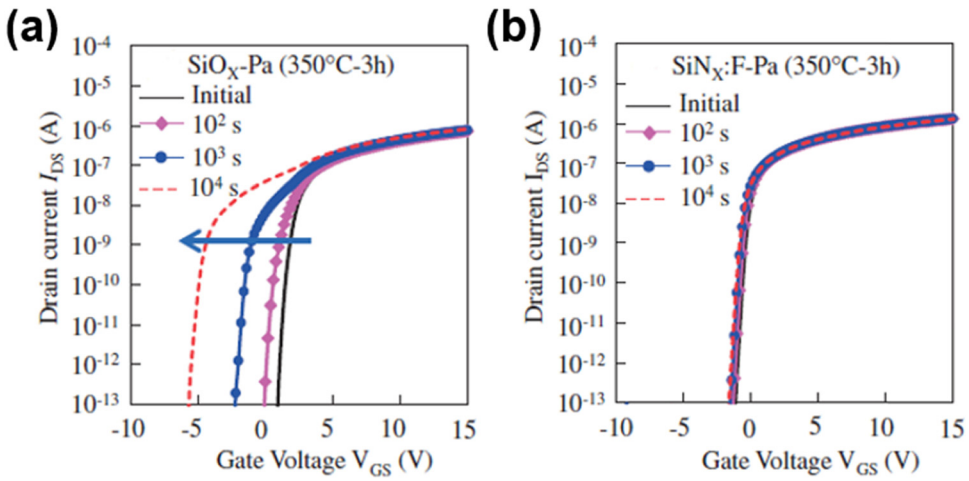

Fig. 16 (a) Changes in transfer characteristics during PBTS of 100 °C for the a-IGZO TFTs with (a) SiOx and (b) SiNx:F passivations after N_2 annealing at 350 °C for 3 h. Copyright 2014 American Institute of Physics. Reproduced with permission from ref. 114.

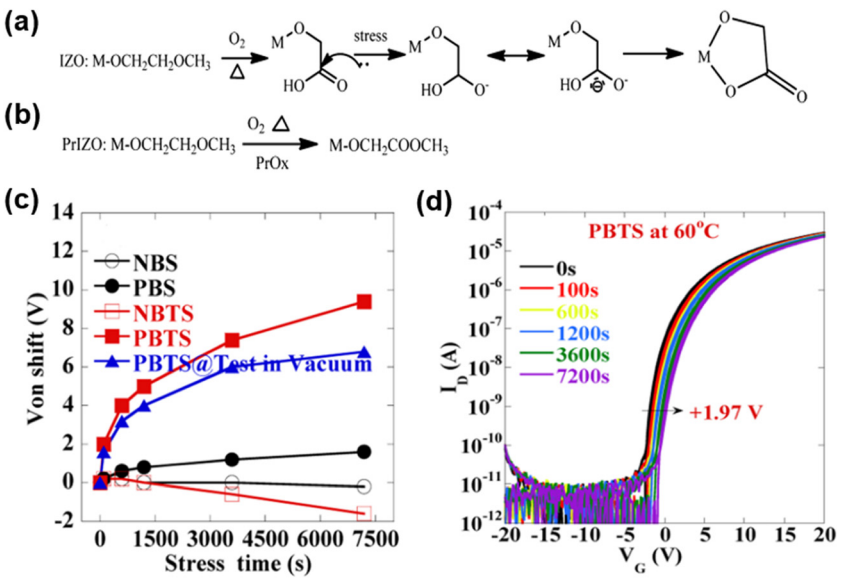

Fig. 17 Electron-withdrawing characteristics during PBTS measurement of (a) IZO- and (b) PrIZO-based TFTs. Bias stability test of (c) alcoholysis-processed IZO-TFTs and PrIZO-TFT under PBTS at 60 °C in air ambient. Copyright 2018 American Chemical Society. Reproduced with permission from ref. 115.

of 10^4 s at 100 °C (Fig. 16(a)). On the other hand, the a-IGZO device with SiN_X:F passivation exhibited highly stable operation with a V_{th} shift of only 0.45 V under the same PBTS condition (Fig. 16(b)).

Similar to the studies mentioned above, Li *et al.* employed praseodymium (Pr) as a dopant in indium–zinc oxide (IZO)-based TFTs to investigate the mechanism of thermal stability and enhance PBTS and NBTS stability.[115] Carbon residues remaining in the AOSs after the annealing process could afford poor thermal stability of oxide TFTs.[118] For instance, in the IZO film formed *via* the alcoholysis process, the $-OCH_3$ and $-CH_2-$ (linked to $-OCH_3$) with strong electron-donating properties could easily be oxidized to carboxylic acid groups in high temperatures (Fig. 17(a)). These carboxylic acid groups, which have a strong electron-withdrawing property would trap the electrons and generate the five-membered ring structure, inducing the steric hindrance and tension during thermal stress. On the other hand, for Pr-doped IZO film, the $-OCH_3$ and $-CH_2-$ are hardly oxidized to carboxylic acid groups, affording a more stable ester group with the passivation effect of PrO_X (Fig. 18(b)). As a result, Pr-doped IZO-based TFTs resulted in more stable PBTS performance at 60 °C for 7200 s with a V_{th} shift of 1.97 V, compared to that of undoped IZO-TFTs (ΔV_{th} = 9.52 V) (Fig. 17(c) and (d)).

While oxygen vacancies are a well-known cause of instability in AOSs, they also act as a carrier source of AOSs. Thus, ensuring both high mobility and stability of AOSs can be challenging due to their trade-off relationship.[89] Kim *et al.*

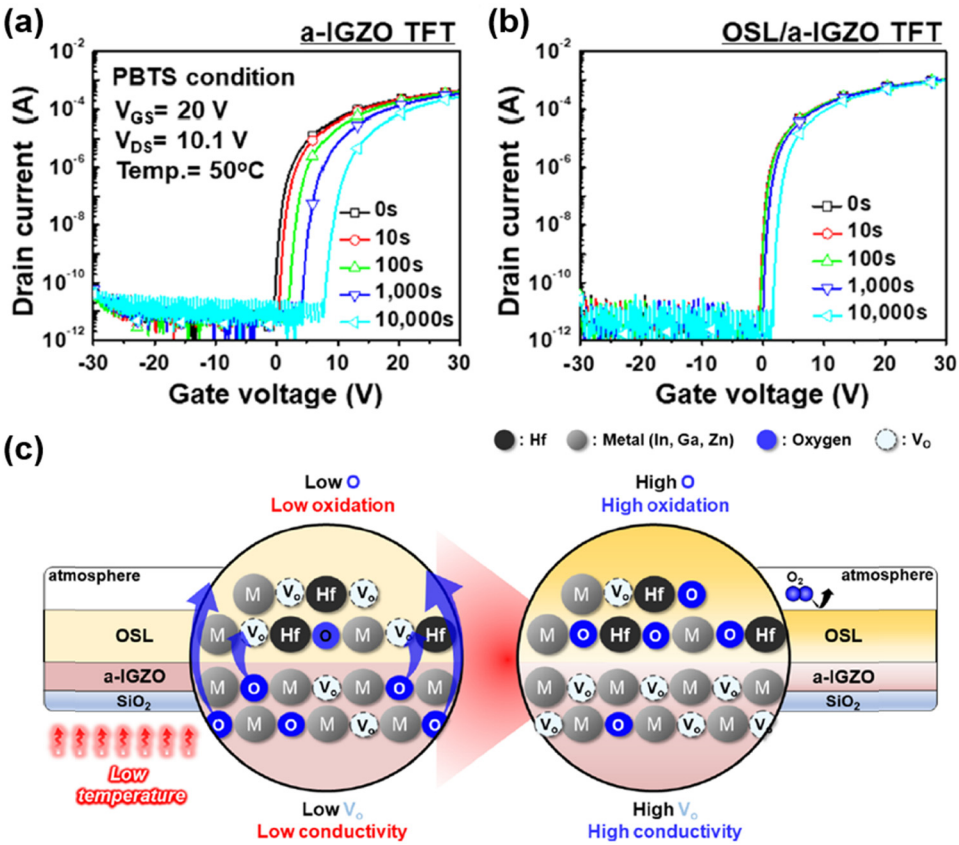

Fig. 18 PBTS test results of the (a) a-IGZO TFT, (b) OSL/a-IGZO TFT, (c) schematic illustration of the oxygen scavenging effect during the annealing process. Copyright 2021 American Chemical Society. Reproduced with permission from ref. 116.

Table 4 Threshold voltage shift and methods to enhance the stability of metal-oxide thin-film transistor under illumination and heat stress

		Stress						
Year	Channel	Temperature (°C)	Light source	Time (s)	Applied voltage (V)	Method	ΔV_{th}[a] (V)	Ref.
2010	GIZO	60	Halogen lamp	10 800	−20		−3.5	123
	GIZO	60	Halogen lamp	10 800	−20	Deposition of ES[b] layer	−0.8	
2013	IGZO	60	White LED, 2000 lux		−20		−7.94	124
	IGZO	60	White LED, 2000 lux		−20	Water vapor condition	−3.36	
	IGZO	60	White LED, 2000 lux		−20	High pressure water vapor condition	−1.96	

[a] Threshold voltage shift (ΔV_{th}) during stress. [b] Etch-stopper.

proposed a new fabrication method that introduces an oxygen scavenger layer (OSL) on AOS to ensure high mobility and stability even at a low-temperature annealing process.[116] In their study, the authors employed Hf-doped a-IGZO layer as the OSL because of its ability to absorb oxygen ions from the AOS, owing to the high oxygen bonding strength of Hf. PBTS tests (V_G = 20 V, V_{DS} = 10.1 V, 50 °C) were performed to investigate the effect of the OSL on the a-IGZO layer. Whereas the V_{th} shift of an a-IGZO layer was 9.22 V (Fig. 18(a)), the V_{th} shift of an OSL/a-IGZO TFT was 2.31 V (Fig. 18(b)). The PBTS stability was improved by reduced V_O concentration of back channel, which easily attracts surrounding oxygen ions compared to a-IGZO TFTs (Fig. 18(c)).[119,120] Thus, V_O, which acts as a carrier source, increases in the a-IGZO layer as the Hf ions in the OSL absorb the oxygen ions.[121] In addition, decreasing V_O in the OSL would prevent the adsorption of oxygen molecules from ambient air. As a result, the OSL/a-IGZO TFT concurrently exhibited high mobility and high PBTS stability.

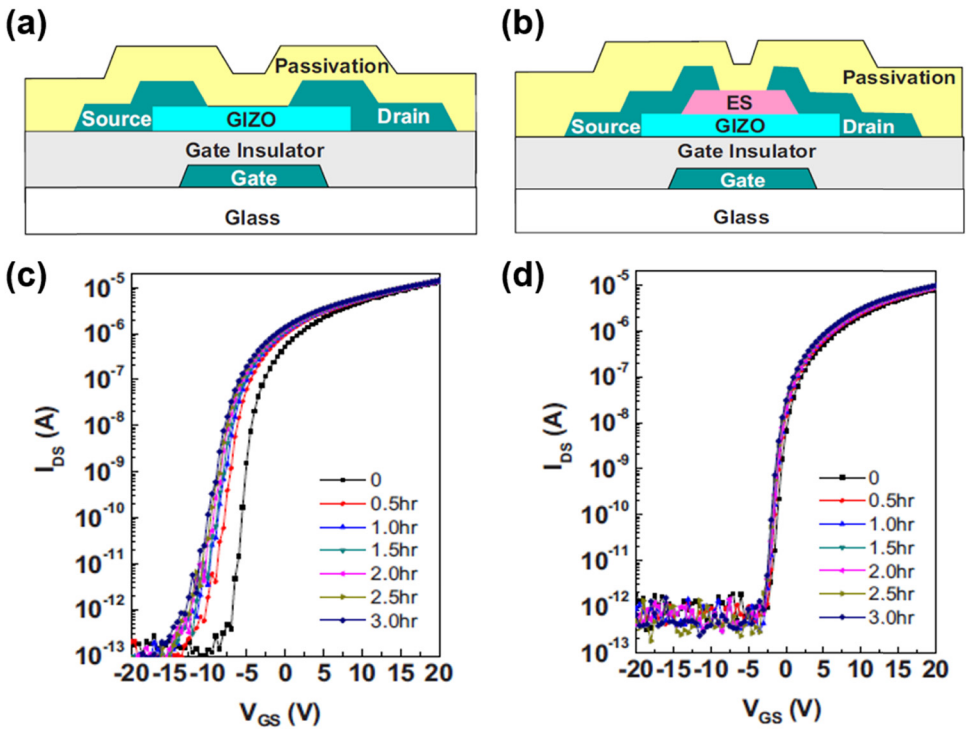

Fig. 19 Schematic cross-section of the GIZO TFTs (W/L = 70/20 μm), which have an inverted staggered bottom-gate structure with (a) back-channel-etch (BCE) and (b) etch stopper (ES) configuration. Evolutions of the transfer curves as a function of the applied NBTIS time for the (c) BCE and (d) ES configurations. Copyright 2010 The Institute of Physics Publishing. Reproduced with permission from ref. 123.

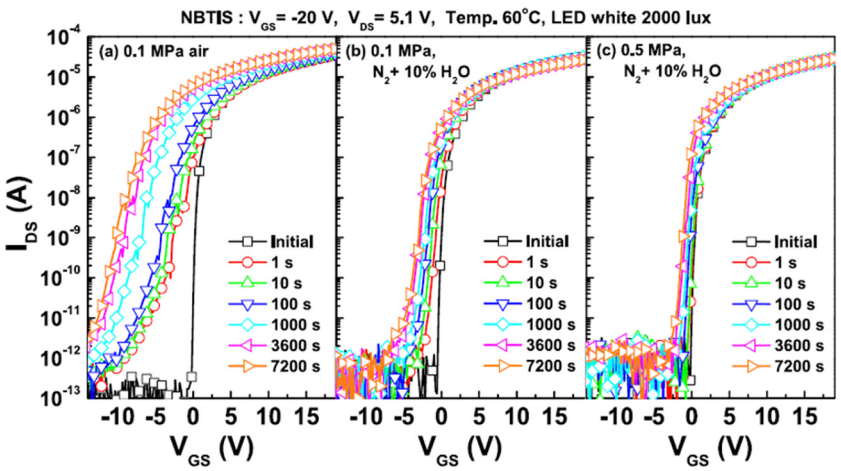

Fig. 20 NBTIS results of a-IGZO TFTs for the post-annealing condition of (a) air at 0.1 MPa, (b) N_2 + H_2O (10%) at 0.1 MPa, and (c) N_2 + H_2O (10%) at 0.5 MPa. Copyright 2013 American Institute of Physics. Reproduced with permission from ref. 124.

5. Stress induced by illumination and heat

While display devices are in operation, TFTs are generally exposed to light illumination from the backlight at a temperature relatively higher than room temperature. Stress induced by illumination on AOS TFTs tends to generate free electrons mediated by the defect states and photoionized oxygen vacancies.[122] At the same time, thermal stress could induce more defects relatively easily.[122] Hence, due to the stress of both illumination and heat, AOS TFTs would be severely damaged. Although AOS TFTs often experience both of these stresses simultaneously, there are few studies that describe the combined effect of these stresses on AOS TFTs and the methods to overcome them for enhanced stability of the resulting devices (Table 4).[123,124]

Kwon *et al.* employed an etch-stopper (ES) layer for Ga–In–Zn–O (GIZO) TFTs to improve device stability under negative bias thermal stress with light.[123] The GIZO TFT device fabricated with a back-channel-etch (BCE) process (Fig. 19(a)) adopts a simple fabrication process but is vulnerable to plasma damage during the dry-etch process. Thus, TFTs with BCE configuration tend to exhibit more structural defects and undesired carrier trap states.[125] To prevent these issues, the ES layer was introduced to protect the GIZO channel layer (Fig. 19(b)). In terms of the film morphology, a rough interfacial layer was observed between the channel and passivation layer in the GIZO device without the ES layer, while a smooth layer was formed in the ES type device (not shown). As a result, the TFT with a BCE configuration showed a large negative shift of 3.5 V in the V_{th} value with degradation in SS value under negative-bias temperature illumination stress (NBTIS) (Fig. 19(c)). On the other hand, the TFT with ES configuration showed highly stable operation with a V_{th} shift of only 0.8 V without any deterioration in the SS value (Fig. 19(d)).

Rim *et al.* proposed that a combined annealing method using water vapor and high pressure could improve the stability and reduce the hump phenomenon of a-IGZO TFTs under NBTIS.[124] Under the water vapor and high-pressure annealing conditions, water molecules can efficiently diffuse and penetrate into the a-IGZO film, passivating defects such as oxygen vacancies in the a-IGZO films.[94,126] The reduction of oxygen vacancy formed by diffused water vapor would lead to the reduction of the photo-induced transition from neutral oxygen vacancy to ionized oxygen vacancy under NBTIS. Furthermore, this could reduce the hump phenomenon observed in transfer characteristics of AOS TFTs under NBTIS tests. As shown in Fig. 20, the a-IGZO TFT annealed at high-pressure (0.5 MPa) under 10% water vapor conditions exhibited a lower ΔV_{th} value of −1.96 V under NBTIS for 2 h than that annealed at 0.1 MPa (ΔV_{th} = −7.94 V) under ambient air or that annealed at relatively low pressure (0.1 MPa) (ΔV_{th} = −3.36 V).

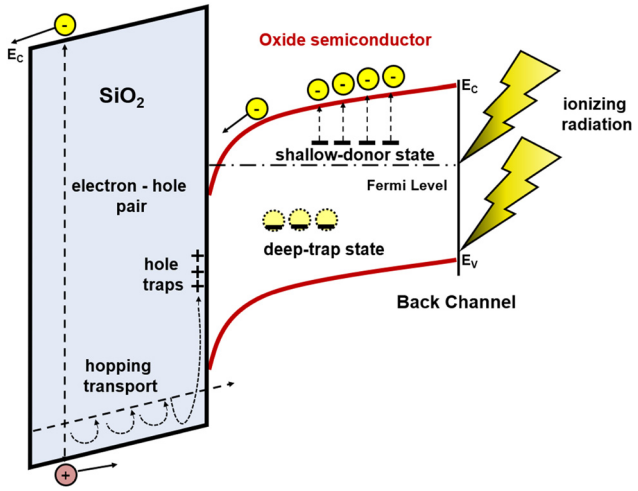

Fig. 21 The scheme of degradation mechanism of AOS under ionizing radiation stress.

6. Stress induced by ionizing radiation

Electronic devices are often used in harsh environments such as the medical, space, and energy industries.[127] As a result, it is

Table 5 Threshold voltages shift and methods to enhance the stability of metal-oxide thin-film transistors under ionizing radiation stress

		Radiation					
Year	Channel	Type	Beam energy	Dose	Method	ΔV_{th}[a] (V)	Ref.
2016	GIZO	X-ray	17.5 keV	410 krad	Dielectric thickness control (385 nm)	−5.6	137
	GIZO	X-ray	17.5 keV	410 krad	Dielectric thickness control (114 nm)	−1.1	
2018	IGZO	Proton	5 meV	10^{14} Dose		−93.8	138
	ZTO	Proton	5 meV	10^{15} Dose	ZTO semiconductor	−6.3	
	ZTO	Proton	5 meV	10^{15} Dose	PCBM Passvation	5	
2020	IWO	Co-60 source		1000 krad	Doping W (2%)	−6.90	139
	IWO	Co-60 source		1000 krad	Doping W (4%)	−4.70	
	IWO	Co-60 source		1000 krad	Doping W (6%)	−3.50	
2021	IGTO	Proton	5 meV	10^{13} Dose	Film thickness control (42 nm)		140
	IGTO	Proton	5 meV	10^{13} Dose	Film thickness control (27 nm)	−5.9[b] (ΔV_{on})	
	IGTO	Proton	5 meV	10^{13} Dose	Film thickness control (12 nm)	−0.5[b] (ΔV_{on})	
2021	InO_X	Gamma-ray	662 keV	103 krad	ZrLaO gate dielectric	0.16	141

[a] Threshold voltage shift (ΔV_{th}) during stress. [b] Turn-on voltage shift (ΔV_{on}) during stress.

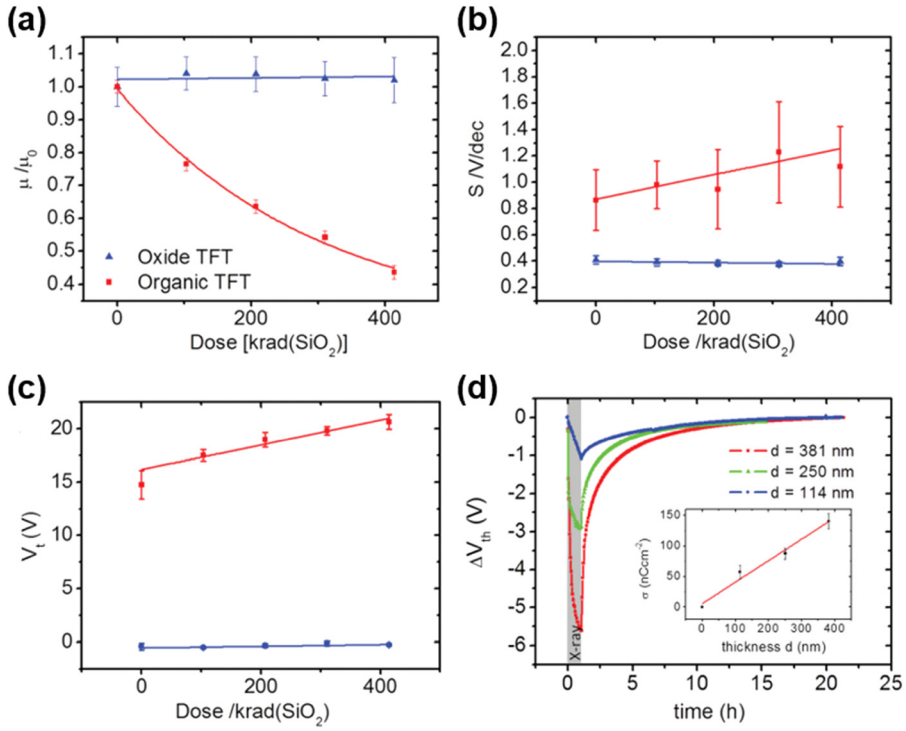

Fig. 22 Transport parameters of flexible transistors based on oxide or organic semiconductor as a function of total X-ray exposure dose: (a) mobility normalized to the unexposed device, μ_0/μ; (b) subthreshold slope S; (c) threshold voltage V_{th}. Error bars show the standard variation measured in a batch ($N > 5$) of transistors, (d) threshold voltage shift and recovery process for oxide transistors containing dielectric layers of varying thicknesses (381, 250, and 114 nm). Copyright 2016 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. Reproduced with permission from ref. 137.

unavoidable that these devices would be exposed to ionizing radiation, such as high-energy photons and particles. Ionizing radiation induces the electrical degradation of AOS TFTs due to the formation of semiconductor channel defects, structural

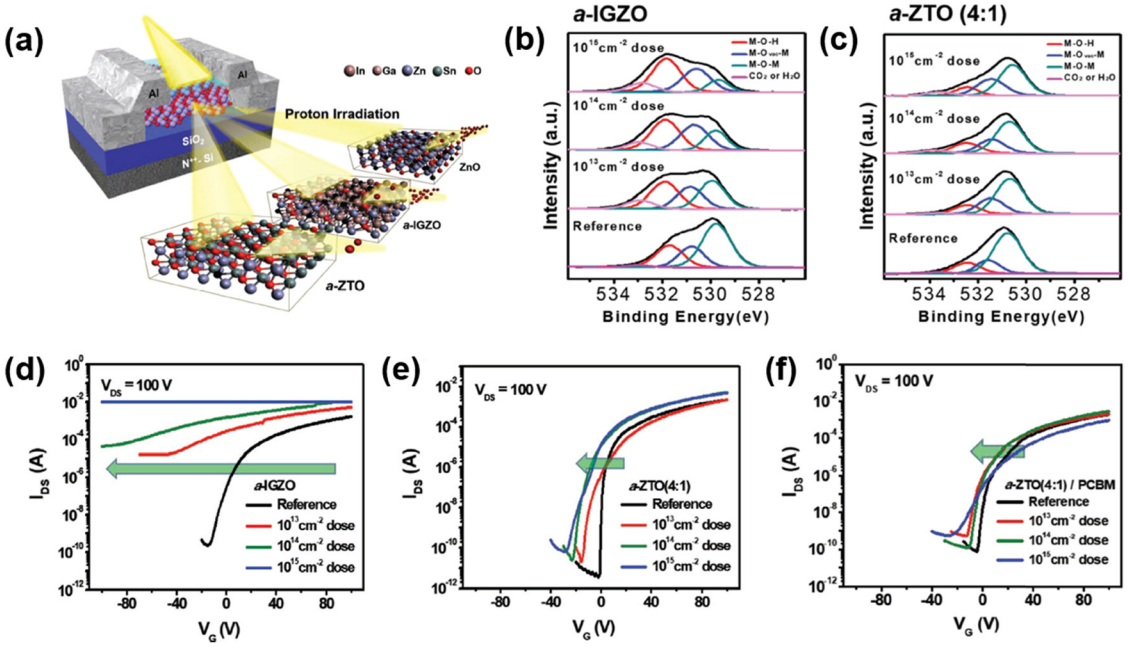

Fig. 23 (a) Schematic of high-energy proton irradiation on oxide semiconductor TFTs (a-ZTO, a-IGZO, ZnO), XPS O1s spectra of oxide semiconductor films before and after various doses of 5 MeV proton irradiation for (b) a-IGZO, (c) a-ZTO (4 : 1), Transfer curves of (d) a-IGZO, (e) a-ZTO (4 : 1), and (f) a-ZTO(4 : 1)/PCBM thin-film transistors before and after 5 MeV proton irradiation dose of 10^{13}, 10^{14}, and 10^{15} cm^{-2}. Copyright 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. Reproduced with permission from ref. 138.

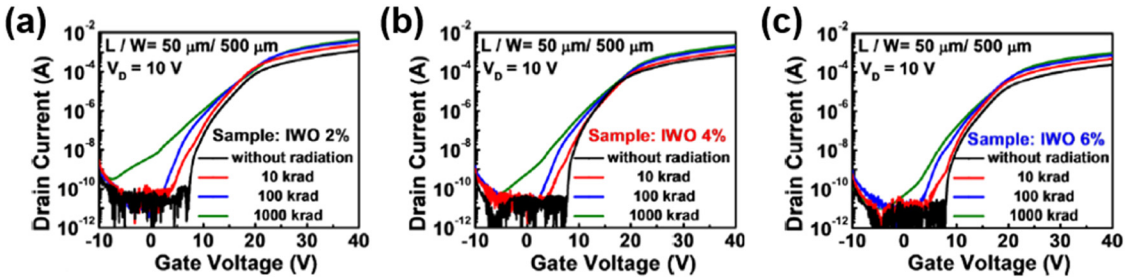

Fig. 24 (a) The transfer characteristics of a-IWO TFT devices with different WO_3 contents under various total dosages of ionizing radiation exposure: (a) IWO 2%, (b) IWO 4%, and (c) IWO 6%. Copyright 2020 American Institute of Physics. Reproduced with permission from ref. 139.

disorder, and trapped charges at the gate dielectric and semiconductor–dielectric interface.[128–130] The dominant radiation-induced channel defects are known to be oxygen vacancies.[131] Oxygen vacancies formed by radiation would act as shallow-donor states and/or deep-trap states.[19] Shallow-donor states near the CBM can generate excessive carriers and cause threshold voltage shift,[132,133] while deep-trap states at the band-tail and mid-gap can capture holes and electrons for a long period of time, affording an increase in subthreshold swing (SS) and carrier mobility.[134] Besides the TFT channel defects, high-energy ionizing radiation could induce the generation of electron–hole pairs in the gate dielectric layer and afford localized trap states in the dielectric and semiconductor–dielectric interface, resulting in the degradation of device performance (Fig. 21).[77,135,136] There have been a few recent efforts to diminish/prevent the degradation of AOS TFTs under ionizing radiation stress (Table 5).[137–141]

To prevent the degradation of AOS TFTs by X-ray radiation exposure, radiation-hardened fully flexible TFT with a GIZO and a multilayer high-k dielectric Ta_2O_5/SiO_2 was introduced by Cramer *et al.*[137] To assess radiation hardness, the TFTs were exposed to photons emitted from a Mo X-ray at a dose rate of 1.5 krad min^{-1} (SiO_2). As shown in Fig. 22, the GIZO-based TFT retained its high electrical performance, such as mobility, V_{th}, and SS, compared to the organic TFT under X-ray exposure. Furthermore, the effect of radiation exposure on various thicknesses (114, 250, and 381 nm) of gate insulator was also investigated (Fig. 22(d)). During exposure to X-ray irradiation, the smallest decrease in V_{th} (−1.1 V) was observed for the TFT with the thinnest insulator, while the device with the thickest insulator showed a V_{th} change of −5.6 V. The number of charged traps in the gate insulator would increase with the thickness of the dielectric as more highly energetic X-ray photons were absorbed.[142]

In 2018, our group investigated the effect of the atomic composition of various AOSs against proton radiation and developed a highly-stable oxide semiconductor, a-ZTO, with an optimized Zn : Sn (4 : 1) ratio (Fig. 23(a)).[138] High-energy proton collision with AOS results in oxygen vacancy generation in semiconductors, which leads to the formation of shallow donor states and deep trap states. X-ray photoemission spectroscopy (XPS) analysis showed that a-ZTO (4 : 1) generated fewer oxygen vacancies than a-IGZO under 5 MeV proton radiation

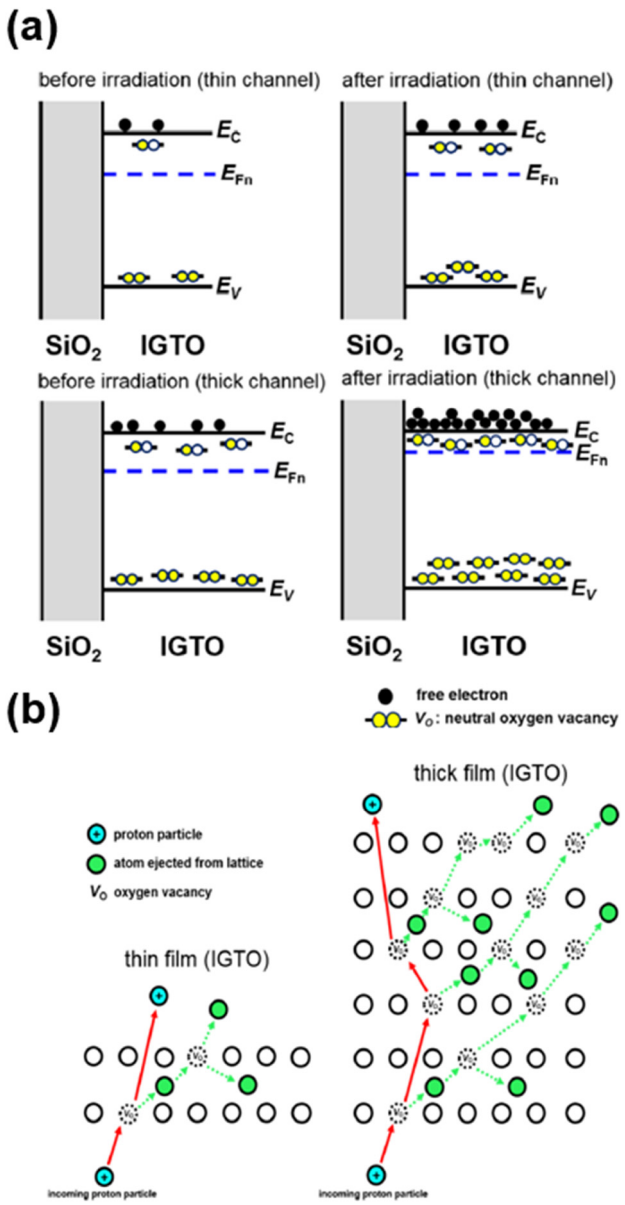

Fig. 25 (a) Schematic energy band diagrams for thin and thick channel IGTO TFTs before and after the proton beam irradiation. (b) Schematic diagram of the mechanism of the larger increase in the V_o concentration in the thicker IGTO thin films after the proton irradiation based on the multiple displacement chain reaction model. Copyright 2021 Elsevier BV. Reproduced with permission from ref. 140.

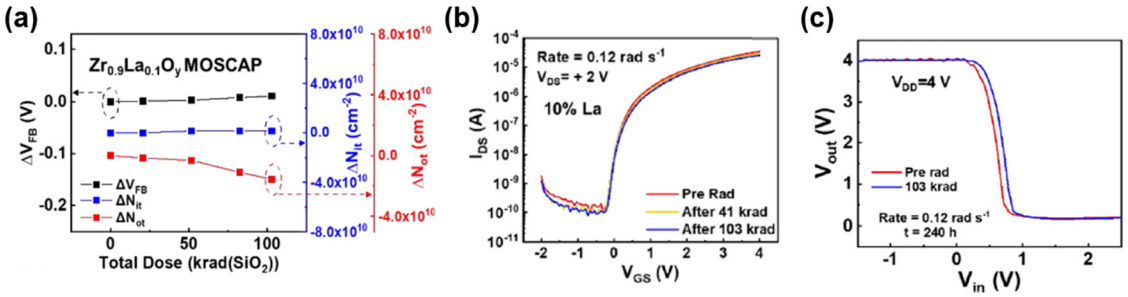

Fig. 26 (a) Summarized shift of flat band-voltage(ΔV_{FB}), oxide trap density (ΔN_{ot}), and interface trap density (ΔN_{it}) of $Zr_{0.9}La_{0.1}O_y$ metal-oxide-semiconductor capacitors (MOSCAPs) after 103 krad irradiation exposure, (b) I_{DS}–V_{GS} before and after 103 krad irradiation of $InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs, (c) voltage transfer characteristic curve of 13 MΩ resistor-loaded inverters (at V_{DD} = 4 V) based on $InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs. Copyright 2021 American Chemical Society. Reproduced with permission from ref. 141.

(Fig. 23(b) and (c)). The structural flexibility of Zn as well as strong Sn–oxygen bonding in ZTO semiconductor seems to have afforded high stability for the resulting device under proton radiation. In the transfer curve, a-ZTO (4 : 1) exhibited stable performance with a ΔV_{th} shift of −6.3 V and a slight increase in mobility compared to a-IGZO under 10^{15} cm^{-2} dose of proton irradiation (Fig. 23(d) and (e)). In addition, back-channel passivation was employed to further saturate the unfilled coordination at the back channel of the oxide and suppress the formation of oxygen vacancies. As shown in Fig. 23(f), a-ZTO (4 : 1) passivated with PCBM exhibited more stable performance with a V_{th} change of <5 V under 10^{15} cm^{-2} dose of proton irradiation.

Ruan *et al.* investigated the effect of tungsten (W)-doping on the radiation hardness of indium oxide TFTs against high-energy ionizing radiation.[139] The channel conductivity and carrier concentration generally increases with increasing ionizing radiation dosage.[143] It is known that tungsten with high oxygen bond dissociation energy could act as an effective carrier suppressor. The active layers of amorphous W-doped indium oxide (a-IWO) film with different WO_3 contents (2 wt%, 4 wt%, and 6 wt%) were fabricated by room-temperature reactive sputtering. As shown in Fig. 24, the a-IWO TFT with 2%, 4%, and 6% WO_3 contents exhibited threshold voltage shifts of 6.90 V, 4.65 V, and 3.50 V, respectively, under 100 krad high dosage ionizing radiation exposure. The TFT with IWO semiconductor film with 4% WO_3 content exhibited higher mobility of 14.49 cm^2 V^{-1} s^{-1} than that of IWO film with 6% WO_3 content (4.74 cm^2 V^{-1} s^{-1}). Therefore, considering the trade-off between mobility and stability, the IWO film with 4% WO_3 content was deemed the optimized AOS under radiation exposure.

Shin *et al.* investigated the effects of channel thickness on proton radiation damage in In–Ga–Sn–O (IGTO) semiconductors.[140] In this experiment, IGTO TFTs with thicknesses of 12, 27, and 42 nm were exposed to 5 MeV proton radiation with a 10^{13} cm^{-2} dose. As mentioned above, an oxygen vacancy (V_O) acts as a shallow donor as well as a deep trap. As shown in Fig. 25(a), the energy diagram of the thick and thin IGTO semiconductors before and after proton radiation indicates that as the film thickness increases, there is a more pronounced increase in the V_O^+ concentration near the CBM. This would induce an increase of electron free carriers that affect electrical performance, such as mobility and V_{th}. When proton particles collide with the IGTO film, the oxygen atoms would eject from the lattice and initiate a multiple displacement chain reaction. This collision would be more severe in thicker AOS film, resulting in the formation of a larger number of vacancy sites (Fig. 25(b)). As a result, the TFT with the thinnest IGTO channel (12 nm) exhibited the highest radiation hardness with a V_{on} shift of −0.5 V under proton radiation of 10^{13} cm^{-2} dose.

Fang *et al.* employed radiation-hardened ZrLaO gate dielectric layers to reduce/prevent defects induced by gamma-ray radiation for indium oxide (InOx) TFTs.[141] Doping of La in ZrO_2 demonstrated better electrical performance of the resulting device with radiation hardness due to the higher La–O bond dissociation energy than that of the Zr–O bond and the suppressed V_O generation in the oxide layer. The $Zr_{0.9}La_{0.1}O_y$-based metal-oxide-semiconductor capacitors (MOSCAPs) exhibited a low flat band-voltage (V_{FB}) sensitivity of 0.11 mV $krad^{-1}$ under low dose and 0.19 mV $krad^{-1}$ under high dose gamma-ray radiation exposure, respectively (Fig. 26(a)). Furthermore, $InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs exhibited a small subthreshold swing (SS) of 0.11 V dec^{-1} and a small interface trap density (D_{it}) of 1×10^{12} cm^{-2}. To identify radiation stability, PBS test was performed for each device after gamma-ray exposure. A small ΔV_{th} was observed under 600 s PBS test after gamma-ray 103 krad exposure (Fig. 26(b)). In addition, $InO_x/Zr_{0.9}La_{0.1}O_y$ TFT-based inverter devices were fabricated with stable operation under gamma-ray radiation (Fig. 26(c)).

7. Conclusion and outlook

For the practical application of display technology at an industrial level, ensuring the stability of AOS TFTs against various external stresses is of great importance. To achieve highly-stable TFTs based on AOSs under various stresses, methods to control the defect states vulnerable to stresses have been investigated widely. This highlight article explores the degradation mechanisms of AOS TFTs under five different types of

stress and introduces several recent approaches to reduce/prevent stress-induced instability. The external stresses are categorized into five groups: (i) voltage bias stress, (ii) illumination stress, (iii) heat stress, (iv) illumination and heat stress, and (v) ionizing radiation stress. The concepts for each category, along with representative examples employed to prevent the degradation induced by each stress, are summarized in Tables 1–5.

Intrinsic structural defects, as well as stress-induced changes, in AOS TFTs have been known to deteriorate the electrical performance of the corresponding devices. Various approaches to reduce/prevent the generation of defect states have been investigated for each external stress. As for the voltage bias stress, gate bias stresses such as PBS and NBS are representative examples, which induce electron traps and migration of ionized oxygen vacancies. To suppress bias stress-induced degradation of the devices, most efforts have focused on the prevention/reduction of defect generation in AOSs. These include controlling oxygen vacancy concentration, doping metal cations to suppress oxygen vacancies, passivating the back-channel, and post-deposition annealing. Illumination stress is inevitable due to the backlight unit in the display pixel array. When AOS TFTs are exposed to light, several processes can occur, including photoionization of oxygen vacancies, generation of electron–hole pairs, and photo-desorption of oxygen from the back channel of AOS. In the illumination stress section, various approaches to enhance the stability of AOSs under illumination, such as the use of passivation, introduction of oxygen vacancy suppressors, reduction of defects *via* cyclic annealing process, and band-gap engineering, were discussed. Thermal stress can damage devices by accelerating electrons, which tend to break chemical bonds and generate defects (mostly oxygen vacancies). Therefore, previous research studies aimed at alleviating the degradation of AOS TFTs caused by heat stress were mainly focused on using dopants such as yttrium, nitrogen, fluorine, and praseodymium to suppress oxygen vacancies. In a real display operation of pixel arrays, both heat and illumination stresses might be applied to TFTs simultaneously. Thus, research efforts to reduce light- and heat-induced defects by using a passivation layer or optimizing annealing conditions have been investigated. In addition, AOS TFTs used for mission-critical applications can be degraded by ionizing radiation in harsh environments. Under ionizing radiation stress, oxygen vacancies are generated in the semiconductor layer and holes are trapped in the dielectric layer and at the semiconductor–dielectric interface. The TFTs based on novel oxide semiconductors and gate dielectrics with optimized thickness and dopants resistant to ionizing radiation have been reported.

So far, previous research on improving the stability of AOS TFT against various external stresses has been successful. While there have been several successful research studies on identifying degradation mechanisms and improving device stability in AOS TFTs, there is currently a lack of quantitative assessment methodologies for their electrical stability. Most research studies have been conducted using their own protocols, which involve varying stress times, irradiation doses, applied voltages, and other parameters. Therefore, it is necessary to systematize the stability assessment index in order to advance towards the high-tech next-generation flat panel display industry. The change in V_{th} value could serve as a metric for assessing the performance index, as it undergoes a significant shift under stress conditions, unlike other electrical parameters such as SS, current on–off ratio, and mobility. Therefore, a systematic approach is required to analyze the stability of various AOS TFTs by considering the dependence of the V_{th} shift on stress times, temperature, irradiation dose, and applied voltage. We expect this highlight to further inspire the standardization of research protocols for analyzing stress-induced degradation, as well as new research for developing highly stable AOS TFTs with high electrical performance.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korean government (MSIT) (RS-2022-00142063).

References

1 H.-W. Chen, J.-H. Lee, B.-Y. Lin, S. Chen and S.-T. Wu, *Light: Sci. Appl.*, 2018, **7**, 17168.
2 H. J. Jang, J. Y. Lee, J. Kwak, D. Lee, J.-H. Park, B. Lee and Y. Y. Noh, *J. Inf. Disp.*, 2019, **20**, 1–8.
3 A. Khazanchi, A. Kanwar, L. Saluja, A. Damara and V. Damara, *Int. J. Comput. Sci. Eng.*, 2012, **1**, 75–84.
4 T. Arai, *J. Soc. Inf. Disp.*, 2012, **20**, 156–161.
5 E. Fortunato, P. Barquinha and R. Martins, *Adv. Mater.*, 2012, **24**, 2945–2986.
6 H. Hosono, *J. Non-Cryst. Solids*, 2006, **352**, 851–858.
7 N. Morosawa, M. Nishiyama, Y. Ohshima, A. Sato, Y. Terai, K. Tokunaga, J. Iwasaki, K. Akamatsu, Y. Kanitani and S. Tanaka, *J. Soc. Inf. Disp.*, 2013, **21**, 467–473.
8 K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano and H. Hosono, *Nature*, 2004, **432**, 488–492.
9 Y. G. Mo, M. Kim, C. K. Kang, J. H. Jeong, Y. S. Park, C. G. Choi, H. D. Kim and S. S. Kim, *J. Soc. Inf. Disp.*, 2011, **19**, 16–20.
10 J. Shi, J. Zhang, L. Yang, M. Qu, D.-C. Qi and K. H. Zhang, *Adv. Mater.*, 2021, **33**, 2006230.
11 J. F. Wager, B. Yeh, R. L. Hoffman and D. A. Keszler, *Curr. Opin. Solid State Mater. Sci.*, 2014, **18**, 53–61.
12 M. Mativenga, D. Geng and J. Jang, *Soc. Inf. Disp. Int. Symp. Tech. Pap.*, 2014, **45**, 1–4.
13 T. Kamiya and H. Hosono, *NPG Asia Mater.*, 2010, **2**, 15–22.
14 T. Kamiya, K. Nomura and H. Hosono, *Sci. Technol. Adv. Mater.*, 2010, **11**, 044305.

15 K. Jenifer, S. Arulkumar, S. Parthiban and J. Kwon, *J. Electron. Mater.*, 2020, **49**, 7098–7111.
16 R. Cross and M. De Souza, *Appl. Phys. Lett.*, 2006, **89**, 263513.
17 L. Petti, N. Münzenrieder, C. Vogt, H. Faber, L. Büthe, G. Cantarella, F. Bottacchi, T. D. Anthopoulos and G. Tröster, *Appl. Phys. Rev.*, 2016, **3**, 021303.
18 D. P. Gosain and T. Tanaka, *Jpn. J. Appl. Phys.*, 2009, **48**, 03B018.
19 S.-H. Hwang, K. Yatsu, D.-H. Lee, I.-J. Park and H.-I. Kwon, *Appl. Surf. Sci.*, 2022, **578**, 152096.
20 Y. Jeong, C. Bae, D. Kim, K. Song, K. Woo, H. Shin, G. Cao and J. Moon, *ACS Appl. Mater. Interfaces*, 2010, **2**, 611–615.
21 J. C. Park, S. W. Kim, S. I. Kim, H. Yin, J. H. Hur, S. H. Jeon, S. H. Park, I. H. Song, Y. S. Park and U. I. Chung, IEEE International Electron Devices Meeting (IEDM), 2009, pp. 1–4.
22 K. Ide, K. Nomura, H. Hosono and T. Kamiya, *Phys. Status Solidi A*, 2019, **216**, 1800372.
23 Y.-M. Kim, K.-S. Jeong, H.-J. Yun, S.-D. Yang, S.-Y. Lee, Y.-C. Kim, J.-K. Jeong, H.-D. Lee and G.-W. Lee, *Appl. Phys. Lett.*, 2013, **102**, 173502.
24 P.-T. Liu, C.-H. Chang and C.-J. Chang, *Appl. Phys. Lett.*, 2016, **108**, 261603.
25 J. K. Jeong, H. Won Yang, J. H. Jeong, Y.-G. Mo and H. D. Kim, *Appl. Phys. Lett.*, 2008, **93**, 123508.
26 T. Kamiya, K. Nomura and H. Hosono, *J. Disp. Technol.*, 2009, **5**, 273–288.
27 H. Oh, S.-M. Yoon, M. K. Ryu, C.-S. Hwang, S. Yang and S.-H. K. Park, *Appl. Phys. Lett.*, 2010, **97**, 183502.
28 S. Jin, T.-W. Kim, Y.-G. Seol, M. Mativenga and J. Jang, *IEEE Electron Device Lett.*, 2014, **35**, 560–562.
29 J. H. Jeong, H. W. Yang, J.-S. Park, J. K. Jeong, Y.-G. Mo, H. D. Kim, J. Song and C. S. Hwang, *Electrochem. Solid-State Lett.*, 2008, **11**, H157.
30 L.-Y. Su, H.-Y. Lin, H.-K. Lin, S.-L. Wang, L.-H. Peng and J. Huang, *IEEE Electron Device Lett.*, 2011, **32**, 1245–1247.
31 Y. Jeong, K. Song, D. Kim, C. Y. Koo and J. Moon, *J. Electrochem. Soc.*, 2009, **156**, H808.
32 M. A. Marrs, C. D. Moyer, E. J. Bawolek, R. J. Cordova, J. Trujillo, G. B. Raupp and B. D. Vogt, *IEEE Trans. Electron Device*, 2011, **58**, 3428–3434.
33 I.-T. Cho, J.-M. Lee, J.-H. Lee and H.-I. Kwon, *Semicond. Sci. Technol.*, 2008, **24**, 015013.
34 S. Lim, J.-M. Kim, D. Kim, S. Kwon, J.-S. Park and H. Kim, *J. Electrochem. Soc.*, 2009, **157**, H214.
35 A. Suresh and J. Muth, *Appl. Phys. Lett.*, 2008, **92**, 033502.
36 J. Troughton and D. Atkinson, *J. Mater. Chem. C*, 2019, **7**, 12388–12414.
37 D. Ho, H. Jeong, S. Choi and C. Kim, *J. Mater. Chem. C*, 2020, **8**, 14983–14995.
38 M. D. H. Chowdhury, M. Mativenga, J. G. Um, R. K. Mruthyunjaya, G. N. Heiler, T. J. Tredwell and J. Jang, *IEEE Trans. Electron Device*, 2015, **62**, 869–874.
39 J. F. Conley, *IEEE Trans. Device Mater. Reliab.*, 2010, **10**, 460–475.
40 J.-S. Park, J. K. Jeong, H.-J. Chung, Y.-G. Mo and H. D. Kim, *Appl. Phys. Lett.*, 2008, **92**, 072104.
41 D. Ho, H.-Y. Jeong, M. N. Le, H. Usta, H.-I. Kwon, M.-G. Kim and C. Kim, *J. Mater. Chem. C*, 2020, **8**, 11209–11222.
42 Y. J. Tak, S. T. Keene, B. H. Kang, W.-G. Kim, S. J. Kim, A. Salleo and H. J. Kim, *ACS Appl. Mater. Interfaces*, 2019, **12**, 2615–2624.
43 J. S. Park, T. S. Kim, K. S. Son, K.-H. Lee, W.-J. Maeng, H.-S. Kim, E. S. Kim, K.-B. Park, J.-B. Seon and W. Choi, *Appl. Phys. Lett.*, 2010, **96**, 262109.
44 A. de Jamblinne de Meux, A. Bhoolokam, G. Pourtois, J. Genoe and P. Heremans, *Phys. Status Solidi A*, 2017, **214**, 1600889.
45 H.-K. Noh, K.-J. Chang, B. Ryu and W.-J. Lee, *Phys. Rev. B: Condens. Matter Mater. Phys.*, 2011, **84**, 115205.
46 J. S. Park, K. Kim, Y. G. Park, Y. G. Mo, H. D. Kim and J. K. Jeong, *Adv. Mater.*, 2009, **21**, 329–333.
47 H.-W. Park, A. Song, S. Kwon, B. Du Ahn and K.-B. Chung, *Appl. Phys. Express*, 2016, **9**, 111101.
48 A. Abliz, L. Xu, D. Wan, H. Duan, J. Wang, C. Wang, S. Luo and C. Liu, *Appl. Surf. Sci.*, 2019, **475**, 565–570.
49 B.-Y. Su, S.-Y. Chu, Y.-D. Juang and S.-Y. Liu, *J. Alloys Compd.*, 2013, **580**, 10–14.
50 P. He, H. Xu, L. Lan, C. Deng, Y. Wu, Y. Lin, S. Chen, C. Ding, X. Li and M. Xu, *Comm. Mater.*, 2021, **2**, 86.
51 D. Wan, X. Liu, A. Abliz, C. Liu, Y. Yang, W. Wu, G. Li, J. Li, H. Chen and T. Guo, *IEEE Trans. Electron Device*, 2018, **65**, 1018–1022.
52 L. Lan, N. Xiong, P. Xiao, M. Li, H. Xu, R. Yao, S. Wen and J. Peng, *Appl. Phys. Lett.*, 2013, **102**, 242102.
53 L. Lan, C. Ding, P. He, H. Su, B. Huang, J. Xu, S. Zhang and J. Peng, *Nanomaterials*, 2022, **12**, 3902.
54 L. Lan, X. Li, C. Ding, S. Chen, H. Su, B. Huang, B. Chen, H. Zhou and J. Peng, *Adv. Electron. Mater.*, 2022, **8**, 2200187.
55 S. Parthiban and J.-Y. Kwon, *J. Mater. Res.*, 2014, **29**, 1585–1596.
56 M. Li, L. Lan, M. Xu, H. Xu, D. Luo, P. Xiao and J. Peng, *Solid-State Electron.*, 2014, **91**, 9–12.
57 N. Tiwari, R. N. Chauhan, P.-T. Liu and H.-P. D. Shieh, *RSC Adv.*, 2016, **6**, 75693–75698.
58 S.-Y. Huang, T.-C. Chang, M.-C. Chen, S.-W. Tsao, S.-C. Chen, C.-T. Tsai and H.-P. Lo, *Solid-State Electron.*, 2011, **61**, 96–99.
59 T. Kamiya, K. Nomura, M. Hirano and H. Hosono, *Phys. Status Solidi C*, 2008, **5**, 3098–3100.
60 K. Hoshino, D. Hong, H. Q. Chiang and J. F. Wager, *IEEE Trans. Electron Device*, 2009, **56**, 1365–1370.
61 C.-J. Ku, W.-C. Hong, T. Mohsin, R. Li, Z. Duan and Y. Lu, *IEEE Electron Device Lett.*, 2015, **36**, 914–916.
62 S. Li, M. Wang, D. Zhang, H. Wang and Q. Shan, *IEEE J. Electron Devices Soc.*, 2019, **7**, 1063–1071.
63 S.-P. Jeon, J. S. Heo, I. Kim, Y.-H. Kim and S. K. Park, *ACS Appl. Mater. Interfaces*, 2020, **12**, 57996–58004.
64 T. Kamiya and H. Hosono, *ECS Trans.*, 2013, **54**, 103.
65 J. W. Jin, A. Nathan, P. Barquinha, L. Pereira, E. Fortunato, R. Martins and B. Cobb, *AIP Adv.*, 2016, **6**, 085321.

66 M. G. Yun, Y. K. Kim, C. H. Ahn, S. W. Cho, W. J. Kang, H. K. Cho and Y.-H. Kim, *Sci. Rep.*, 2016, **6**, 31991.
67 J. Liu, D. B. Buchholz, J. W. Hennek, R. P. Chang, A. Facchetti and T. J. Marks, *J. Am. Chem. Soc.*, 2010, **132**, 11934–11942.
68 K. S. Karim, A. Nathan, M. Hack and W. I. Milne, *IEEE Electron Device Lett.*, 2004, **25**, 188–190.
69 K. Kim, S. Jeon, H. Lee, M. Seo, H. Cho and B. Choi, *ECS J. Solid State Sci. Technol.*, 2019, **8**, Q3242.
70 J. Y. Bak, S. Yang, M. K. Ryu, S. H. Ko Park, C. S. Hwang and S. M. Yoon, *ACS Appl. Mater. Interfaces*, 2012, **4**, 5369–5374.
71 S.-B. Seo, H.-S. Park, J.-H. Jeon, H.-H. Choe, J.-H. Seo, S. Yang and S.-H. K. Park, *Thin Solid Films*, 2013, **547**, 263–266.
72 D. Wang, M. P. Hung, J. Jiang, T. Toda and M. Furuta, *ACS Appl. Mater. Interfaces*, 2014, **6**, 5713–5718.
73 D. Wang, M. P. Hung, J. Jiang, T. Toda and M. Furuta, *ECS Trans.*, 2014, **64**, 65.
74 H.-J. Lee, S. H. Cho, K. Abe, M.-J. Lee and M. Jung, *Sci. Rep.*, 2017, **7**, 1–9.
75 T. Song, D. Zhang, M. Wang, H. Wang and Y. Yang, *IEEE Trans. Electron Devices*, 2021, **68**, 2742–2747.
76 T. Takahashi, M. N. Fujii, R. Miyanaga, M. Miyanaga, Y. Ishikawa and Y. Uraoka, *Appl. Phys. Express*, 2020, **13**, 054003.
77 H.-J. Lee, K. Abe, H. Y. Noh, J.-S. Kim, H. Lee and M.-J. Lee, *Sci. Rep.*, 2019, **9**, 1–9.
78 H.-J. Lee and K. Abe, *IEEE Electron Device Lett.*, 2020, **41**, 896–899.
79 J. H. Park, Y.-g Kim, S. Yoon, S. Hong and H. J. Kim, *ACS Appl. Mater. Interfaces*, 2014, **6**, 21363–21368.
80 D. J. Kim, Y. S. Rim and H. J. Kim, *ACS Appl. Mater. Interfaces*, 2013, **5**, 4190–4194.
81 J.-S. Seo and B.-S. Bae, *ACS Appl. Mater. Interfaces*, 2014, **6**, 15335–15343.
82 H. Y. Jung, Y. Kang, A. Y. Hwang, C. K. Lee, S. Han, D.-H. Kim, J.-U. Bae, W.-S. Shin and J. K. Jeong, *Sci. Rep.*, 2014, **4**, 1–8.
83 J. C. Park and H.-N. Lee, *IEEE Electron Device Lett.*, 2012, **33**, 818–820.
84 E. Kim, C.-K. Kim, M. K. Lee, T. Bang, Y.-K. Choi, S.-H. K. Park and K. C. Choi, *Appl. Phys. Lett.*, 2016, **108**, 182104.
85 J. Lee, H. Kim, T. Park, Y. Ko, J. Ryu, H. Jeon, J. Park and H. Jeon, *J. Vac. Sci. Technol., A*, 2012, **30**, 01A104.
86 G. Kwon, K. Kim, B. D. Choi, J. Roh, C. Lee, Y. Y. Noh, S. Seo, M. G. Kim and C. Kim, *Adv. Mater.*, 2017, **29**, 1607055.
87 J. Jeong, G. Jun Lee, J. Kim and B. Choi, *Appl. Phys. Lett.*, 2012, **100**, 112109.
88 K. Nomura, T. Kamiya and H. Hosono, *Appl. Phys. Lett.*, 2011, **99**, 053505.
89 Y.-S. Shiah, K. Sim, Y. Shi, K. Abe, S. Ueda, M. Sasase, J. Kim and H. Hosono, *Nat. Electron.*, 2021, **4**, 800–807.
90 N. Singh, C. Yan and P. S. Lee, *Sens. Actuators, B*, 2010, **150**, 19–24.
91 K. H. Ji, J.-I. Kim, Y.-G. Mo, J. H. Jeong, S. Yang, C.-S. Hwang, S.-H. K. Park, M.-K. Ryu, S.-Y. Lee and J. K. Jeong, *IEEE Electron Device Lett.*, 2010, **31**, 1404–1406.
92 J. K. Jeong, *J. Mater. Res.*, 2013, **28**, 2071–2084.
93 K. Ghaffarzadeh, A. Nathan, J. Robertson, S. Kim, S. Jeon, C. Kim, U.-I. Chung and J.-H. Lee, *Appl. Phys. Lett.*, 2010, **97**, 143510.
94 K. H. Ji, J.-I. Kim, H. Y. Jung, S. Y. Park, R. Choi, U. K. Kim, C. S. Hwang, D. Lee, H. Hwang and J. K. Jeong, *Appl. Phys. Lett.*, 2011, **98**, 103509.
95 S. Yang, D.-H. Cho, M. K. Ryu, S.-H. K. Park, C.-S. Hwang, J. Jang and J. K. Jeong, *Appl. Phys. Lett.*, 2010, **96**, 213511.
96 E. Sundholm, R. Presley, K. Hoshino, C. Knutson, R. Hoffman, D. Mourey, D. Keszler and J. Wager, *IEEE Electron Device Lett.*, 2012, **33**, 836–838.
97 D. Kang, H. Lim, C. Kim, I. Song, J. Park, Y. Park and J. Chung, *Appl. Phys. Lett.*, 2007, **90**, 192101.
98 M. G. Yun, C. H. Ahn, S. W. Cho, S. H. Kim, Y. K. Kim and H. K. Cho, *ACS Appl. Mater. Interfaces*, 2015, **7**, 6118–6124.
99 Y.-H. Kim, J.-S. Heo, T.-H. Kim, S. Park, M.-H. Yoon, J. Kim, M. S. Oh, G.-R. Yi, Y.-Y. Noh and S. K. Park, *Nature*, 2012, **489**, 128–132.
100 K. Nomura, T. Kamiya, H. Ohta, M. Hirano and H. Hosono, *Appl. Phys. Lett.*, 2008, **93**, 192107.
101 L.-F. Teng, P.-T. Liu, Y.-J. Lo and Y.-J. Lee, *Appl. Phys. Lett.*, 2012, **101**, 132901.
102 H.-C. Chen, T.-C. Chang, W.-C. Lai, G.-F. Chen, B.-W. Chen, Y.-J. Hung, K.-J. Chang, K.-C. Cheng, C.-S. Huang and K.-K. Chen, *ACS Appl. Mater. Interfaces*, 2018, **10**, 25866–25870.
103 J. Gan, X. Lu, J. Wu, S. Xie, T. Zhai, M. Yu, Z. Zhang, Y. Mao, S. C. I. Wang and Y. Shen, *Sci. Rep.*, 2013, **3**, 1–7.
104 Y. Ueoka, Y. Ishikawa, J. P. Bermundo, H. Yamazaki, S. Urakawa, M. Fujii, M. Horita and Y. Uraoka, *ECS J. Solid State Sci. Technol.*, 2014, **3**, Q3001.
105 H. Xu, M. Xu, M. Li, Z. Chen, J. Zou, W. Wu, X. Qiao, H. Tao, L. Wang and H. Ning, *ACS Appl. Mater. Interfaces*, 2019, **11**, 5232–5239.
106 B. Ryu, H.-K. Noh, E.-A. Choi and K.-J. Chang, *Appl. Phys. Lett.*, 2010, **97**, 022108.
107 J. Kim, J. Bang, N. Nakamura and H. Hosono, *APL Mater.*, 2019, **7**, 022501.
108 H. Hosono, *Jpn. J. Appl. Phys.*, 2013, **52**, 090001.
109 J.-M. Lee, I.-T. Cho, J.-H. Lee and H.-I. Kwon, *Appl. Phys. Lett.*, 2008, **93**, 093504.
110 H. Im, H. Song, J. Jeong, Y. Hong and Y. Hong, *Jpn. J. Appl. Phys.*, 2015, **54**, 03CB03.
111 J. G. Um, M. Mativenga, P. Migliorato and J. Jang, *J. Appl. Phys.*, 2014, **115**, 134502.
112 T. Jun, K. Song, Y. Jung, S. Jeong and J. Moon, *J. Mater. Chem.*, 2011, **21**, 13524–13529.
113 J. Raja, K. Jang, N. Balaji, W. Choi, T. Thuy Trinh and J. Yi, *Appl. Phys. Lett.*, 2013, **102**, 083505.
114 J. Jiang, T. Toda, M. P. Hung, D. Wang and M. Furuta, *Appl. Phys. Express*, 2014, **7**, 114103.

115 M. Li, W. Zhang, W. Chen, M. Li, W. Wu, H. Xu, J. Zou, H. Tao, L. Wang and M. Xu, *ACS Appl. Mater. Interfaces*, 2018, **10**, 28764–28771.
116 M. S. Kim, H. T. Kim, H. Yoo, D. H. Choi, J. W. Park, T. S. Kim, J. H. Lim and H. J. Kim, *ACS Appl. Mater. Interfaces*, 2021, **13**, 31816–31824.
117 C.-L. Chuang, W.-J. Wang, C.-Y. Wang, W.-H. Tseng and C.-I. Wu, *Electrochem. Solid-State Lett.*, 2012, **15**, H195.
118 C.-H. Choi, S.-Y. Han, Y.-W. Su, Z. Fang, L.-Y. Lin, C.-C. Cheng and C.-H. Chang, *J. Mater. Chem. C*, 2015, **3**, 854–860.
119 P.-T. Liu, Y.-T. Chou and L.-F. Teng, *Appl. Phys. Lett.*, 2009, **95**, 233504.
120 B. Xiao, X. Yu and S. Watanabe, *ACS Appl. Electron. Mater.*, 2019, **1**, 585–594.
121 W. H. Jeong, G. H. Kim, H. S. Shin, B. Du Ahn, H. J. Kim, M.-K. Ryu, K.-B. Park, J.-B. Seon and S. Y. Lee, *Appl. Phys. Lett.*, 2010, **96**, 093503.
122 T.-C. Chen, Y. Kuo, T.-C. Chang, M.-C. Chen and H.-M. Chen, *J. Phys. D Appl. Phys.*, 2017, **50**, 42LT02.
123 J.-Y. Kwon, K. S. Son, J. S. Jung, K.-H. Lee, J. S. Park, T. S. Kim, K. H. Ji, R. Choi, J. K. Jeong and B. Koo, *Electrochem. Solid-State Lett.*, 2010, **13**, H213.
124 Y. Seung Rim, W. Jeong, B. Du Ahn and H. Jae Kim, *Appl. Phys. Lett.*, 2013, **102**, 143503.
125 C. R. Kagan and P. Andry, *Thin-film transistors*, CRC Press, 2003.
126 H. S. Shin, Y. S. Rim, Y. G. Mo, C. G. Choi and H. J. Kim, *Phys. Status Solidi A*, 2011, **208**, 2231–2234.
127 J. Prinzie, F. M. Simanjuntak, P. Leroux and T. Prodromakis, *Nat. Electron.*, 2021, **4**, 243–253.
128 M.-R. Hao, H.-Y. Hu, C.-G. Liao, B. Wang, H.-Y. Kang and H.-M. Zhang, *Microelectron. Reliab.*, 2017, **75**, 69–76.
129 E. Snow, A. Grove and D. Fitzgerald, *Proc. IEEE*, 1967, **55**, 1168–1185.
130 S. Xue, R. Huang, P. Wang, W. Wang, D. Wu, Y. Pei and X. Zhang, *J. Appl. Phys.*, 2009, **105**, 084505.
131 Z. Muhammad, Y. Wang, Y. Zhang, P. Vallobra, S. Peng, S. Yu, Z. Lv, H. Cheng and W. Zhao, *Adv. Mater. Technol.*, 2022, 2200539.
132 Y. Kikuchi, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano and H. Hosono, *Thin Solid Films*, 2010, **518**, 3017–3021.
133 D. Kong, H.-K. Jung, Y. Kim, M. Bae, Y. W. Jeon, S. Kim, D. M. Kim and D. H. Kim, *IEEE Electron Device Lett.*, 2011, **32**, 1388–1390.
134 W. L. Kalb and B. Batlogg, *Phys. Rev. B: Condens. Matter Mater. Phys.*, 2010, **81**, 035327.
135 T. Cramer, I. Fratelli, P. Barquinha, A. Santa, C. Fernandes, F. D'Annunzio, C. Loussert, R. Martins, E. Fortunato and B. Fraboni, *Sci. Adv.*, 2018, **4**, eaat1825.
136 J. R. Schwank, M. R. Shaneyfelt, D. M. Fleetwood, J. A. Felix, P. E. Dodd, P. Paillet and V. Ferlet-Cavrois, *IEEE Trans. Nucl. Sci.*, 2008, **55**, 1833–1853.
137 T. Cramer, A. Sacchetti, M. T. Lobato, P. Barquinha, V. Fischer, M. Benwadih, J. Bablet, E. Fortunato, R. Martins and B. Fraboni, *Adv. Electron. Mater.*, 2016, **2**, 1500489.
138 B. Park, D. Ho, G. Kwon, D. Kim, S. Y. Seo, C. Kim and M. G. Kim, *Adv. Funct. Mater.*, 2018, **28**, 1802717.
139 D.-B. Ruan, P.-T. Liu, K.-J. Gan, Y.-C. Chiu, C.-C. Hsu and S. M. Sze, *Appl. Phys. Lett.*, 2020, **116**, 182104.
140 M.-G. Shin, S.-H. Hwang, H.-S. Cha, H.-S. Jeong, D.-H. Kim and H.-I. Kwon, *Surf. Interfaces*, 2021, **23**, 100990.
141 Y. Fang, C. Zhao, I. Z. Mitrovic and C. Zhao, *ACS Appl. Mater. Interfaces*, 2021, **13**, 50101–50110.
142 H. Hughes and J. Benedetto, *IEEE Trans. Nucl. Sci.*, 2003, **50**, 500–521.
143 J. I. Ramirez, Y. V. Li, H. Basantani, K. Leedy, B. Bayraktaroglu, G. H. Jessen and T. N. Jackson, *IEEE Trans. Nucl. Sci.*, 2015, **62**, 1399–1404.