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Bioelectronic building blocks: low-voltage integrable organic thin-film transistors with a tri-layer gate dielectric design†

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This study presents a novel tri-layer gate dielectric design for organic thin-film transistors, tailored for bioelectronic applications, with improved yield, uniformity, and integrability for systems. The proposed tri-layer structure consists of a buffer layer, a surface-tuning layer, and a high-*k* layer. Experimental results demonstrate a high yield of 93% with a mobility of 0.94 ± 0.07 cm^2 V^{-1} s^{-1} and a threshold voltage of −0.02 ± 0.06 V, using all-photolithographic processes. Such a high device yield achieved by tri-layer design also enables scalable, large-area integration, which is hardly possible in the previous bi-layer design (of which the device yield is 37%). We demonstrated a 1024-channel bioelectronic stimulation array (an analogue system) with 4096 transistors, achieving an output current of 8.86 ± 2.0 μA over a 3 × 3 cm^2 area, as well as several digital circuits, namely, inverters, NAND, NOR, and D flip-flops. This work highlights the importance of creating reliable, low-voltage, and integrable OTFTs as building blocks for bioelectronics, paving the way for future applications in wearable sensors and implantable systems.

New concepts

The novel concept introduced in this study lies in the development of a tri-layer dielectric structure for OTFTs, specifically designed to overcome the challenges of achieving high performance and large-area integration for bioelectronic applications. This approach combines three strategically engineered layers: a buffer layer that mitigates the number of trap states on the charge transport surface, a surface-tuning layer that improves the compatibility for subsequent solution-based processing, and a high-*k* layer that enhances capacitance, resulting in improved transistor performance. The study offers a solution to achieve a high yield in low-voltage integrable OTFTs, which is essential for device-to-circuit implementation. This tri-layer design demonstrates the potential of OTFTs as building blocks for scalable fabrication of complex bioelectronic devices.

Introduction

Bioelectronics is an emerging field that integrates electronic systems with biological systems, offering vast potential for applications such as wearable sensors,[1,2] neural interfaces,[3,4] and implantable systems.[5,6] Transistors act as the fundamental building blocks in electronic systems, which can be integrated into various functional circuits, ranging from digital logic gates[7,8] to analogue amplifiers.[9,10] Traditionally, complementary metal oxide semiconductor (CMOS)[11–15] technology has dominated the design of electronic systems due to its reliability and high performance. However, the inherent rigidity and limitations in the area scalability of CMOS technology make it unsuitable for large-area and flexible bioelectronic applications. To address these limitations, organic thin-film transistors (OTFTs) have emerged as promising alternatives, offering key advantages including mechanical flexibility, low-cost fabrication, and compatibility with scalable manufacturing.[16–18] Despite these advantages, OTFTs often face challenges such as high operating voltages and difficulties with integration into photolithographic processes.[19] Overcoming these hurdles is essential for realizing the full potential of OTFTs as bioelectronic building blocks.[20–22]

Currently, significant efforts have been made to optimise the performance of OTFTs. One strategy is to utilise small-molecule semiconductors.[23–25] Small-molecule materials typically exhibit higher mobility[26] due to their better ordered and crystalline structures, allowing for lower operating voltages compared to polymers.[27] However, the circuit integration of small-molecule

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OTFTs is often hindered by challenges in uniformity and scalability,[28] as their deposition processes, for example, drop-casting[29] or blade-coating,[30] can lead to significant variations in crystal orientation. Polymer semiconductors, due to their amorphous structure, are more uniform over a large area,[31] making them ideal candidates for building blocks in bioelectronics.[32] However, their disordered molecular structure often results in high threshold voltages, which can pose safety concerns for biological systems.

To enhance device performance in OTFTs with reduced threshold voltages,[33,34] increasing the unit-area capacitance of gate dielectrics is another effective strategy. A higher unit-area capacitance strengthens the electric field for a given gate voltage, enhancing the modulation of charge carriers in the semiconductor channel and lowering the voltage required for equivalent current. The unit-area capacitance is primarily determined by the dielectric constant (k) of the material and the thickness of the gate dielectric.[35,36] Although conventional high-k metal oxides can increase unit-area capacitance, their deposition processes require high temperatures that exceed the thermal budget for flexible substrates, such as polyimide (PI), polyethylene terephthalate (PET) and parylene,[37,38] and organic semiconductors. In contrast, organic high-k dielectrics are promising alternatives, offering potential for improved compatibility with solution-based processing, making them ideal for enhancing the performance of OTFTs.[39,40] Li *et al.*[41] demonstrated the use of poly(vinylidene fluoride-trifluoroethylene-chlorofluoroethylene) (P(VDF-TrFE-CFE)) as a high-k dielectric in solution-processable OTFTs to achieve low-voltage operation. However, the presence of random dipoles in the high-k dielectric introduces trap states, capturing charge carriers and reducing mobility.[42] To address this, Tang *et al.*[43] introduced CYTOP as a buffer layer, focusing on its ability to screen the dipole field of the high-k dielectric on the semiconductor. Although this approach improved device mobility by mitigating trap states, the low surface energy of the CYTOP layer results in poor wettability[44] of the P(VDF-TrFE-CFE) dielectric solution, thus affecting its film uniformity and potentially lowering device yield in solution processing. In this regard, to build a low-voltage bioelectronic system, it is essential to design a novel dielectric that combines relatively high capacitance with good film uniformity and device yield.

In this study, we propose a tri-layer gate dielectric design for low-voltage and integrable OTFTs. As illustrated in Fig. 1(c–e), each layer serves a distinct purpose. The CYTOP buffer layer acts as a thin barrier between the high-k dielectric and the semiconductor, minimizing the dipole effect and protecting the charge transport interface, while minimizing its influence on the high effective unit-area capacitance. Due to the poor wetting of the buffer layer, we introduce an AlO_x surface-tuning layer, deposited by thermal evaporation, to optimise the surface energy for subsequent solution-based high-k dielectric layer deposition. This method also allows precise control over the thickness of the surface-tuning layer, mitigating its impact on the subsequent fabrication processes. The transistors with the tri-layer gate dielectric demonstrated a high yield of 93%, with a

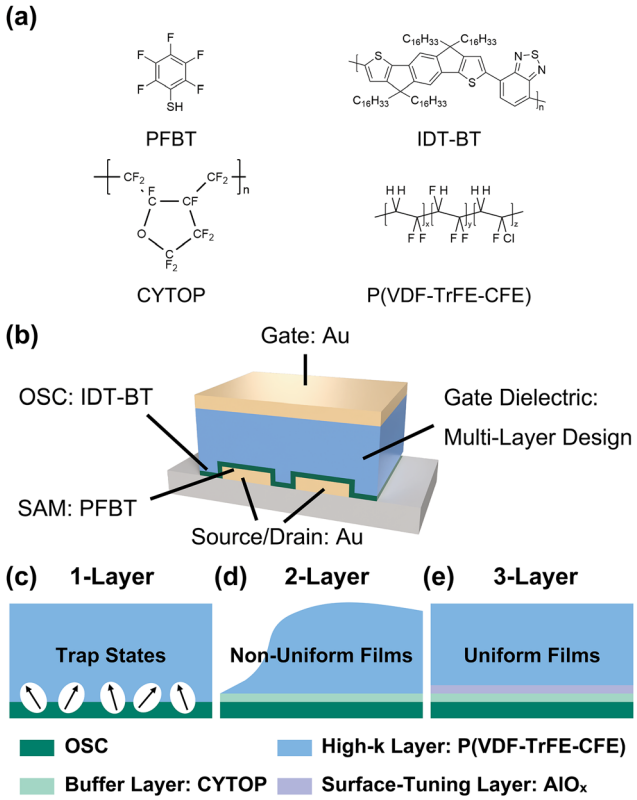

Fig. 1 (a) Chemical structures of key materials and (b) 3D schematic structure of the OTFT. SAM: self-assembled monolayer; OSC: organic semiconductor. Schematic designs of different gate dielectric configurations: (c) mono-layer, (d) bi-layer, and (e) tri-layer.

mobility of 0.94 ± 0.07 $cm^2 V^{-1} s^{-1}$ and a threshold voltage of −0.02 ± 0.06 V. Furthermore, the potential for large-area integration was demonstrated with a 1024-channel stimulation array,[45] incorporating 4096 transistors and achieving an output current of 8.86 ± 2.0 μA over a 3 × 3 cm^2 area. This study emphasises the critical role of dielectric design in enabling low-voltage, integrable building blocks for bioelectronic applications.

Results and discussion

Gate dielectric characterization

As shown in Fig. 2(a), the unit-area capacitance of the mono-layer, bi-layer, and tri-layer structures is 154, 90, and 81 nF cm^{-2} at 10 Hz, respectively. The total thickness of the mono-layer, bi-layer, and tri-layer is 190 nm, 190 nm, and 197 nm, respectively. The capacitance decreases with the addition of more layers. The bi-layer capacitance is largely decreased compared to that of the mono-layer, and the tri-layer capacitance remains nearly identical to that of the bi-layer configuration. For a multi-layer capacitor, the equivalent capacitance (C_{eq}) behaves like that of a series capacitor network,

$$\frac{1}{C_{eq}} = \frac{1}{C_{CYTOP}} + \frac{1}{C_{AlO_x}} + \frac{1}{C_{P(VDF\text{-}TrFE\text{-}CFE)}} \quad (1)$$

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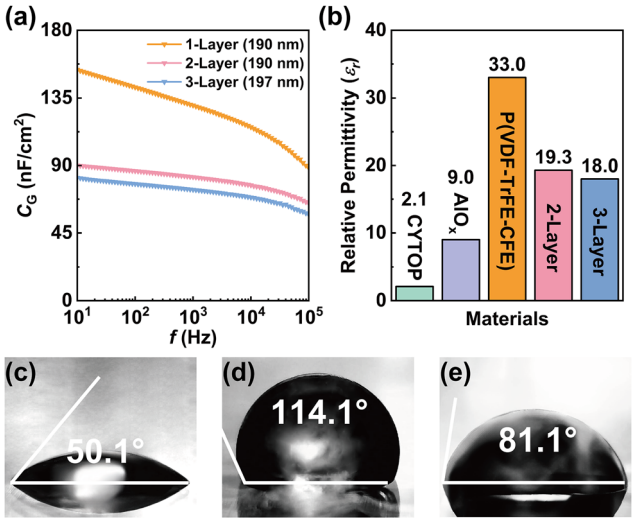

Fig. 2 (a) Unit-area capacitance of different gate dielectric designs as a function of frequency. (b) Intrinsic and effective dielectric constants of different dielectric materials and configurations. (c)–(e) Contact angle images demonstrating the wetting behavior of deionised water on the surfaces of (c) the organic semiconductor, (d) the buffer layer, and (e) the surface tuning layer.

where C_{CYTOP} is the capacitance of the buffer layer, C_{AlO_x} is the capacitance of the surface-tuning layer, and $C_{P(VDF\text{-}TrFE\text{-}CFE)}$ is the capacitance of the high-k layer. In a multi-layer capacitor configuration, the overall capacitance is primarily influenced by the layer with the lowest individual capacitance, making the total value less sensitive to changes in the thickness of other equivalent layers. Among these, the AlO_x layer has minimal impact on the total capacitance due to its relatively high dielectric constant of 9.0 and small thickness of 4.5 nm, and the overall capacitance is dominated by the CYTOP and P(VDF-TrFE-CFE) layers. This makes its capacitance highly sensitive to the thickness of CYTOP and P(VDF-TrFE-CFE) layers, limiting the overall capacitance of the multi-layer structure.

A capacitance decrease with the increase in frequency was also observed in the mono-layer samples. This effect can be primarily attributed to the dielectric dispersion characteristic of P(VDF-TrFE-CFE).[46,47] At low frequencies, the dipoles within the polymer dielectric have sufficient time to align with the oscillating electric field, maximizing their contribution to the overall capacitance. However, as the frequency increases, the dipole alignment lags behind the rapid change in the electric field, resulting in a sharp decrease in effective capacitance. This relaxation effect limits the capacitive performance of this dielectric material at high frequencies, affecting the switching speed and stability of the OTFTs.[48]

Fig. 2(c–e) displays the contact angles of the different dielectric surfaces. We observed the contact angles of 50.1°, 114.1°, and 81.1° for deionised water on the surfaces of IDT-BT, CYTOP, and AlO_x layers, respectively. These results suggest that the addition of the AlO_x layer enhances the wetting properties of the P(VDF-TrFE-CFE) solution, promoting the formation of a P(VDF-TrFE-CFE) dielectric film with better coverage and uniformity. This improvement ensures effective integration of the high-k layer and enhances the overall film quality of the OTFTs during large-scale fabrication, in terms of both chip area and circuit complexity.

Characterization of OTFTs with different gate dielectric designs

Fig. 3(a) shows the photograph of the top-gate bottom-contact p-type OTFT obtained using all-photolithographic processes. The channel width-to-length ratio of the devices was 1500 μm/50 μm. Fig. 3(b) shows that the tri-layer and bi-layer OTFTs exhibit high mobility values of 0.94 ± 0.07 cm^2 V^{-1} s^{-1} and 0.94 ± 0.15 cm^2 V^{-1} s^{-1}, respectively. For mono-layer devices, as the control group in this work, the lower mobility of 0.25 ± 0.01 cm^2 V^{-1} s^{-1} indicates significant mobility degradation with a direct interface between the IDT-BT channel and the high-k dielectric. Due to the random dipoles present at the interfaces, more trap states would be induced, which degrades carrier transport and thus device mobility. The tri-layer OTFTs also demonstrate a steep subthreshold slope (SS) of 0.37 V dec^{-1}, outperforming the bi-layer (0.79 V dec^{-1}) and mono-layer (0.93 V dec^{-1}) devices. The threshold voltages for the tri-layer, bi-layer, and mono-layer devices are −0.02 ± 0.06 V, 0.73 ± 0.21 V, and 2.29 ± 0.33 V, respectively. The degraded SS of the bi-layer devices is mainly due to a high off-state current, which is largely contributed by the high gate leakage current, suggesting poor dielectric quality with uneven film thickness and even pinholes in the absence of the surface tuning layer. Although p-type OTFTs are typically expected to exhibit negative threshold voltages, the devices demonstrate a slightly positive threshold voltage, which may be attributed to the use of a work function material of gold (Au, $\phi \approx 5.1$ eV) as the gate, shifting the threshold voltage positively.[49] How the material selection for the gate electrode affects the threshold voltage can be further investigated in the future work to optimise the device performance. The output characteristics of the tri-layer OTFT, as shown in Fig. 3(c), exhibit a flat and stable output current in the saturation region, with a large early voltage exceeding 100 V. This high early voltage corresponds to a significantly increased output resistance, enabling the transistor to function as an ideal current source.

Fig. 3(d–f) shows the transfer characteristics of all functioning transistors with mono-layer, bi-layer, and tri-layer dielectric configurations. 30 transistors were fabricated on 2-inch substrates. The tri-layer transistors achieve a significantly higher yield of 93% (28/30), outperforming the bi-layer (37%, 11/30) and mono-layer (47%, 14/30) devices. The primary cause of transistor failure is the high gate current, which overwhelms the output current. This issue arises from the inconsistency of the high-k layer on the CYTOP layer, which is the main component of the gate dielectric. The poor quality of the high-k layer can lead to short circuits between the source/drain and the gate. The additional AlO_x layer greatly improves the film quality and insulating properties of the gate dielectric deposition, enhancing the device yield and reliability. A higher transistor yield means fewer failed transistors, which directly translates to a higher circuit yield. For instance, in a circuit with

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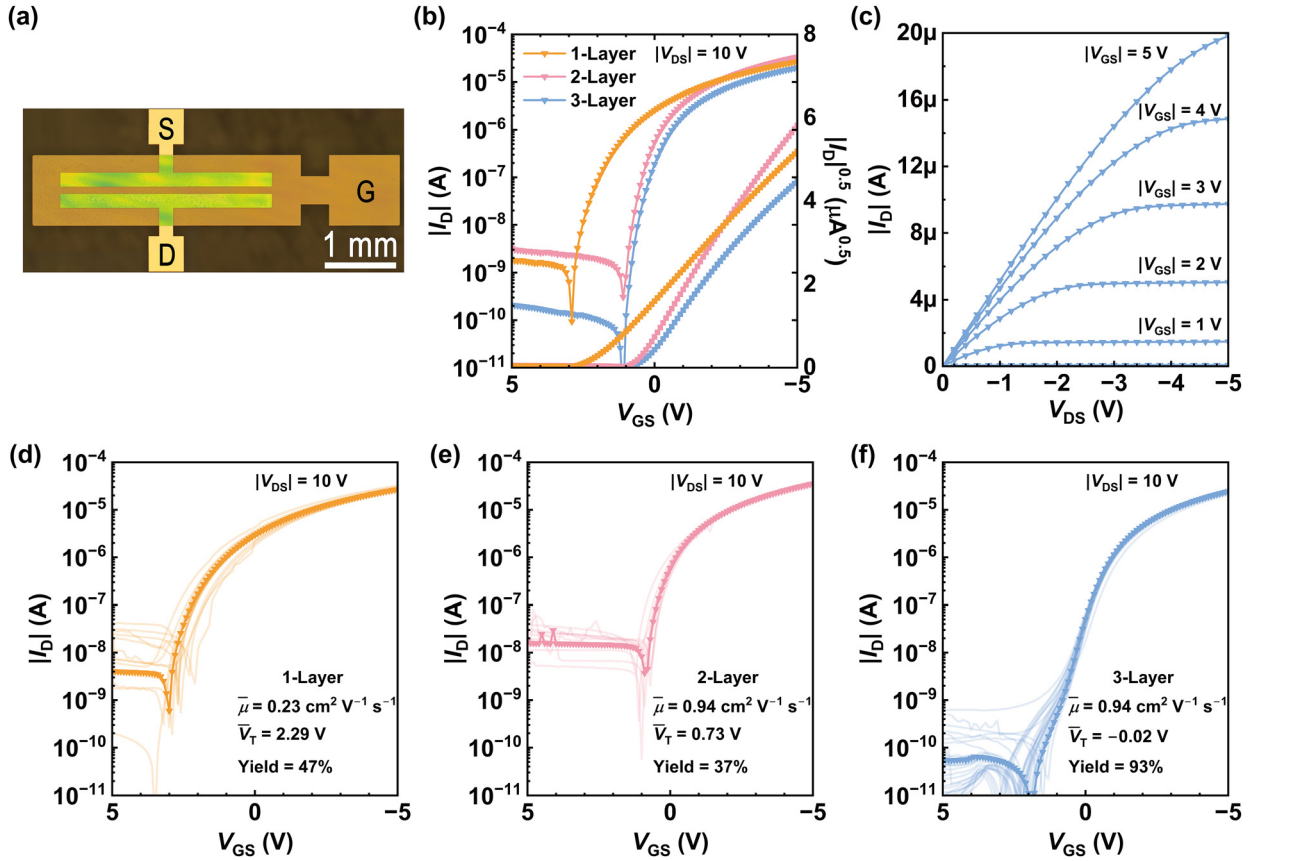

Fig. 3 (a) Microscopic image of the fabricated OTFT. S/D: source/drain region; G: gate region. (b) Comparison of device transfer characteristics for OTFTs with mono-layer, bi-layer, and tri-layer gate dielectrics. (c) Output characteristics of devices with a tri-layer gate dielectric. Transfer characteristics of all functioning devices of a sample with (d) mono-layer, (e) bi-layer, and (f) tri-layer gate dielectrics, showing the variations of device characteristics.

4 transistors, the circuit yield can be estimated using an exponential function of the transistor yield and the number of transistors. The tri-layer devices can provide an estimated circuit yield of 66%, compared to only 1% for the bi-layer devices, which is unacceptable for circuit integration with OTFTs as building blocks. A circuit yield of 66% provides circuit designers with room to improve overall system reliability through redundancy techniques. In contrast, a circuit yield below 1% leaves virtually no room for such design strategies to be effective.

The variation coefficients for mobility are 7%, 16%, and 5% for the tri-layer, bi-layer, and mono-layer transistors, respectively. This indicates that the trap states at the charge transport interface, which significantly impact the intrinsic mobility of the semiconductor,[50] are better mitigated by adding the CYTOP layer at the semiconductor–dielectric interface. Similarly, the standard deviation of the threshold voltage is 0.06 V, 0.21 V, and 0.33 V for the tri-layer, bi-layer, and mono-layer designs, respectively. The uniformity of the threshold voltage is primarily determined by the dielectric layer uniformity and interface trap state density. The CYTOP layer enhances the quality of the semiconductor–dielectric interface, and the AlO_x layer further improves the uniformity of the gate dielectric layer.

The superior yield and uniformity of the tri-layer transistors are critical building blocks for achieving reliable and consistent circuit performance over a large area. This makes the tri-layer structure highly suitable for scalable integration in bioelectronic systems.

The effects of the CYTOP layer and the AlO_x layer

By diluting CYTOP, transistors with different CYTOP layer thicknesses were fabricated. As shown in Fig. 4(a), the thickness decreases while the capacitance increases with decreasing concentration of CYTOP. To achieve low-voltage operation, a larger capacitance is preferred, necessitating a thinner CYTOP layer. This means that a lower concentration of the CYTOP solution is advantageous. However, the transfer characteristics in Fig. 4(b) show that a 7-nm CYTOP layer significantly increases the off-state current for the corresponding OTFTs, primarily due to a large gate leakage current. This leads to a drastically reduced on–off ratio of less than 10^1, compared to values of 10^4–10^5 observed in the devices with thicker CYTOP layers. The inconsistency in the film formed by the CYTOP solutions with lower concentrations disrupts the semiconductor interface, and the dangling bonds of the AlO_x layer further degrade the charge transport properties at the interface. Thus, determining the optimal thickness of the CYTOP layer requires balancing the benefit of higher capacitance from a thinner layer with the need to maintain a stable, uniform film to enhance device performance.

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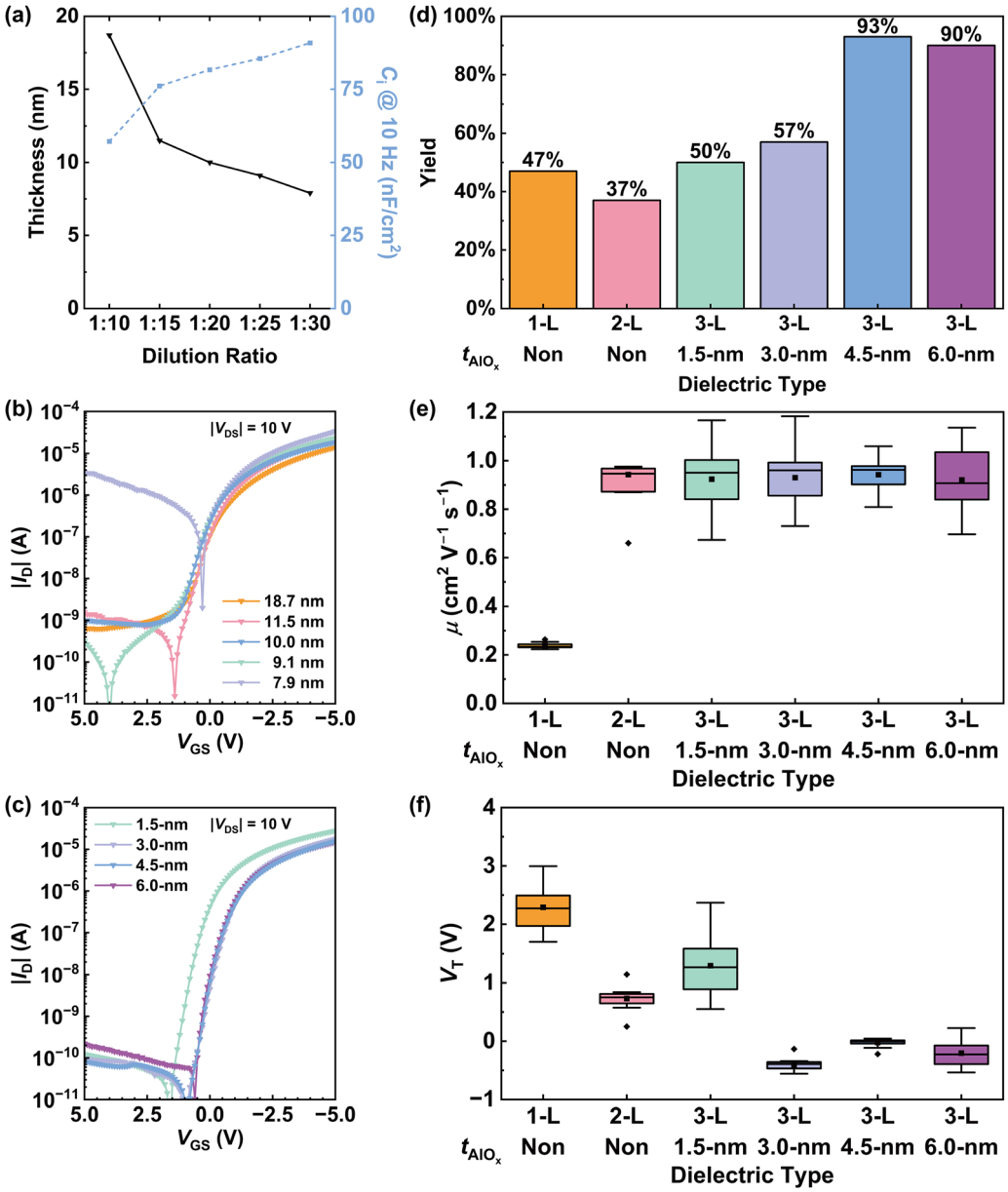

Fig. 4 (a) Relationship between the CYTOP thickness and the equivalent capacitance of the gate dielectric at 10 Hz, for different CYTOP solution concentrations. (b) Transfer characteristics of tri-layer OTFTs with varying CYTOP layer thicknesses. (c) Transfer characteristics of tri-layer OTFTs with different AlO_x layer thicknesses. (d) Yield of 30 transistors fabricated with different dielectric configurations. Distribution of (e) mobility and (f) threshold voltage for functioning devices with different dielectric structures. 1-L means mono-layer devices; 2-L means bi-layer devices; 3-L means tri-layer devices.

Similarly, by adjusting the thickness of the evaporated Al that later naturally oxidised to AlO_x,[51] OTFTs with AlO_x of various thicknesses were fabricated. As shown in Fig. 4(c), the on-state current of the devices decreases as the thickness of the AlO_x layer increases. This is due to the reduction in the equivalent capacitance of the tri-layer dielectric, which is measured to be 84, 83, 82, and 80 nF cm^{-2} for different AlO_x layer thicknesses. The capacitance does not change significantly with the change in the AlO_x thickness, which is in line with the theoretical prediction that the AlO_x layer has minimal impact on the total capacitance. Fig. 4(d) shows the yield of 30 transistors fabricated on 2-inch substrates with different dielectric configurations. A dramatic increase in yield is observed between the 3.0 nm and 4.5 nm thicknesses, which is attributed to the enhanced surface tuning effect with increasing thickness. The contact angle of deionised water on the surface of the AlO_x layer was observed to decrease as the layer thickness increased. This indicates that as the thickness of the AlO_x layer increases, the surface energy also increases, which improves the wetting of the high-k solution. Thicknesses above 4.5 nm show minimal improvement in surface wetting, suggesting that 4.5 nm would be sufficient to provide better

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adhesion for the high-k layer and form a good gate dielectric film without significant pinholes or defects. This facilitates the fabrication process to be reliable and repeatable, and improves the quality of the high-k layer, resulting in higher yield for transistors with AlO_x thickness over 4.5 nm.

The variation coefficients for the mobility of devices with different AlO_x thicknesses were 14%, 14%, 7%, and 14%, as shown in Fig. 4(e), and the standard deviations of the threshold voltage were 0.52 V, 0.01 V, 0.06 V, and 0.21 V, as shown in Fig. 4(f). The optimal uniformity is observed at 4.5 nm AlO_x thickness. The improved uniformity with increased thickness is due to better wetting of the high-k layer, and the decreased uniformity at 6 nm thickness can be attributed to the excessive thickness of the AlO_x layer, hindering semiconductor patterning during wet etching. Therefore, optimizing the surface-tuning layer involves a balance between enhancing surface energy and minimizing the impact on subsequent fabrication steps.

Demonstration of a bioelectronic stimulation array

With the developed OTFTs that possess high yield and uniformity simultaneously, we successfully demonstrated a bioelectronic stimulation array using a four-mask integration process, entirely based on photolithographic patterning. The array consists of 4096 transistors and 1024 capacitors, arranged in a 32 × 32 matrix. As shown in Fig. 5(a), the drive transistor (T2, Fig. 5(a)) acts as the current source to directly stimulate neurons connected to the output electrode, and the other transistors function as switches to control the write-in and output phases of the circuit. Without counting the fan-out wires, the effective area of the array is 3 × 3 cm^2, as shown in Fig. 5(b), highlighting the potential of our OTFTs with the tri-layer gate dielectric design for large-area fabrication. To verify the functionality of the array, we randomly selected and focused on a 5 × 5 unit, which demonstrated a 96% yield, confirming a reliable and consistent fabrication process. The output current was measured to be 8.86 ± 2.0 μA at an operating voltage of 10 V, with a variation of 22%. The decrease in uniformity compared to individual transistors is primarily due to the complexity of the circuit design and fabrication, including the *via* resistance between different metal layers and the IR drop in the array layout.

Fig. 5(e) shows the measured timing diagram of the functioning units. The stimulation intensity is input through the data line and stored in the capacitor. The selection line (V_{Sel}) refreshes the array by selecting each row, and once all the stimulation information is updated, the control line (V_{Ctrl}) triggers synchronised output current across all units. The output current is only observed when the control line activates the control transistor (T3), ensuring that the background current noise is nearly zero and preventing unintended stimulation on neurons.

This demonstration highlights the potential of the tri-layer OTFT building blocks in creating scalable, low-voltage, and

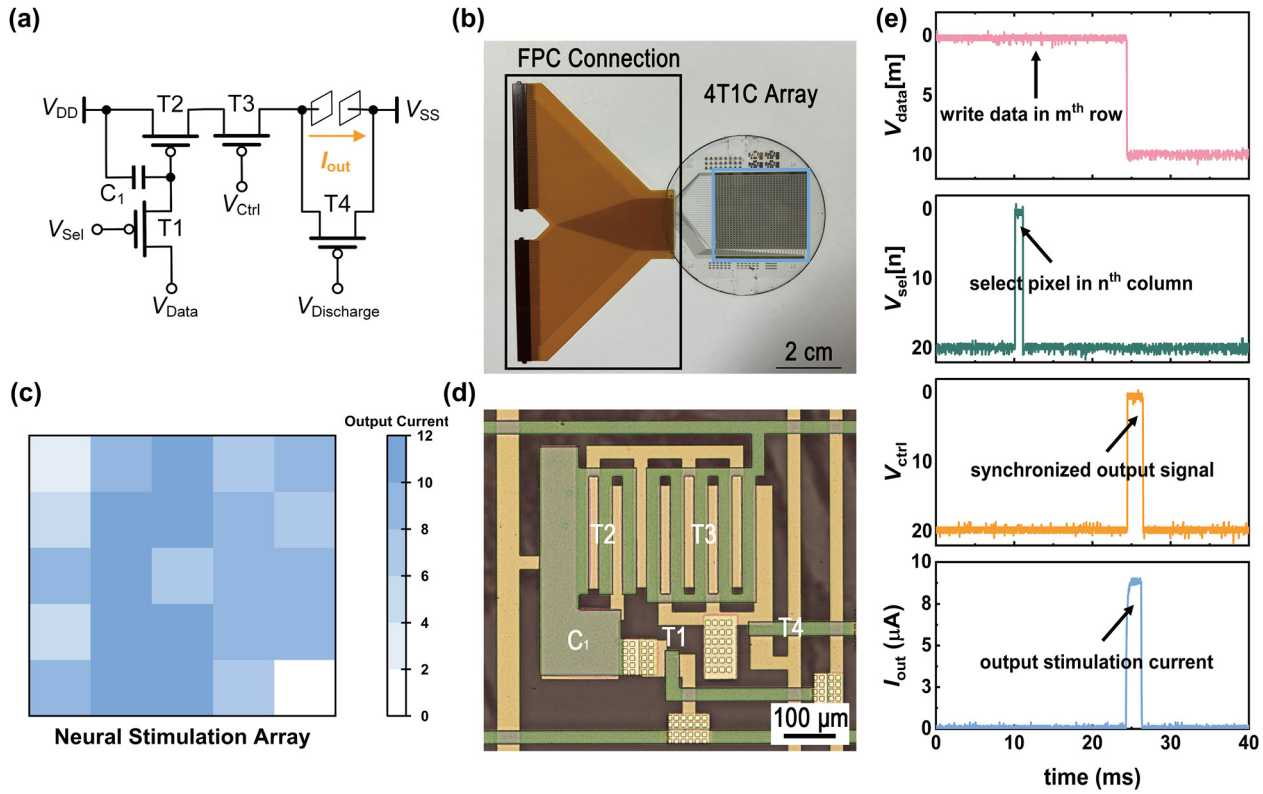

Fig. 5 (a) Schematic design of the 2-inch stimulation array unit with 4 transistors and 1 capacitor. (b) Photograph of the fabricated stimulation array on a 2-inch glass substrate. (c) Heatmap of output currents from a selected area of the stimulation array. (d) Microscopic image of an individual stimulation array unit. (e) Timing diagram illustrating the operation of the stimulation array.

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integrable bioelectronic systems for large-area applications. Apart from the large-area stimulation array as an analogue system, this integration strategy is also promising in digital systems, with the demonstration of logic gate circuits, including inverters, NAND gates, NOR gates and D flip-flops (Fig. S4–S7, ESI†).

Conclusions

This study introduces a novel tri-layer dielectric design for OTFT building blocks, tailored for bioelectronic applications, emphasizing improvements in yield, uniformity, and integration. The careful optimization of buffer, surface tuning, and high-*k* layers significantly enhances transistor performance by protecting the charge transport surface, improving film uniformity, and increasing capacitance, respectively. Such a systematic optimization route is also applicable to other dielectric materials and device technologies. By varying the thickness of each layer, we identified that optimizing the CYTOP layer requires balancing equivalent capacitance with reliable film formation, and the AlO_x layer optimization involves a trade-off between surface energy tuning and minimizing damage on subsequent processes. The reliable fabrication process enables the tri-layer devices with both high yield and good uniformity, making them suitable as building blocks for large-area integration into electrical circuits and systems. Additionally, the successful demonstration of a bioelectronic stimulation array with 4096 transistors ensures the potential of these tri-layer dielectric transistors for scalable, low-power bioelectronic systems. This work highlights the importance of optimizing dielectric structures in OTFTs for large-area bioelectronics, paving the way for next-generation devices in applications such as wearable sensors, flexible displays, and implantable systems.

Methods

Chemicals and materials

For the self-assembled monolayer on the source/drain (S/D) electrodes, a solution of 2,3,4,5,6-pentafluorothiophenol (PFBT, Sigma-Aldrich) in isopropanol was prepared at a concentration of 0.03% (v/v). The active semiconducting layer was formed using a 2.5 mg mL^{-1} solution of indacenodithiophene-*co*-benzothiadiazole (IDT-BT, Derthon) in chlorobenzene, which was magnetically stirred for at least 3 hours to ensure complete dissolution of the semiconductor solutes in chlorobenzene.

The tri-layer dielectric was constructed with CYTOP (AGC Chemicals) as the buffer layer, aluminium oxide (AlO_x) as the surface tuning layer, and P(VDF-TrFE-CFE) (67%/26%/7%, Arkema Piezotech) as the high-*k* layer. The CYTOP was diluted in a 1 : 20 ratio, and a 35 mg mL^{-1} solution of P(VDF-TrFE-CFE) in 2-butanol was prepared.

Device fabrication

The fabrication of OTFTs began with the deposition of a 10-nm chromium (Cr) adhesion layer and a 40-nm gold (Au) layer as the S/D electrodes. The substrates were cleaned using ultraviolet/ozone (UV/O_3) treatment for 15 minutes to enhance the surface properties of the electrodes. The samples were immersed in a PFBT solution for 30 minutes to improve charge injection at the metal–semiconductor interface. The organic semiconductor layer, IDT-BT, was spin-coated at 2500 rpm and annealed at 100 °C for 30 minutes. Next, the CYTOP dielectric layer was spin-coated at 2500 rpm and annealed at 80 °C for 30 minutes in a vacuum environment. A thin layer of Al was thermally evaporated and naturally oxidised by exposing the samples to the air for 8 hours before the following processes. A 180-nm P(VDF-TrFE-CFE) layer was then spin-coated at 2500 rpm and annealed at 100 °C for 3 hours. The gate electrodes were formed by depositing a 50-nm Au layer. All metal layers for the source, drain, and gate electrodes were patterned using photolithography and wet etching. Finally, the device patterns were defined using reactive-ion etching, with the gate electrode serving as the hard mask to remove excess semiconductor and dielectric areas. To measure the gate dielectric layer capacitance, capacitors use the metal–insulator–metal structure with different material combinations, namely, Al/P(VDF-TrFE-CFE)/Al, Al/CYTOP/P(VDF-TrFE-CFE)/Al, and Al/CYTOP/AlO_x/P(VDF-TrFE-CFE)/Al, and with different material thicknesses.

Characterization

The thicknesses of the CYTOP and AlO_x films were measured using an atomic force microscope (FastScan, Bruker). The thicknesses of the P(VDF-TrFE-CFE) and overall gate dielectric films were measured with a surface profiler (Dektak 150, Bruker). The capacitance of the gate dielectric was measured using an LCR meter (IM3533-01, HIOKI). The electrical characteristics of the OTFTs were analysed with a semiconductor parameter analyser (B1500A, Keysight). The mobility and threshold voltage were extracted using the linear extrapolation method in the saturation region. The stimulation array was controlled by a microcontroller (ATmega2560, Arduino). The output current was measured using a current–voltage amplifier (SR470, Stanford Research) and recorded on a digital oscilloscope (DSOX2024A, Keysight).

Conflicts of interest

The authors declare no conflicts of interest.

Data availability

All data are presented in the main text or the ESI.†

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