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New concepts:

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COMMUNICATION

High-Temperature Negative Differential Resistance in Tungsten Diselenide Multilayers without Heterojunctions

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Various exotic functional electronics devices have been proposed to address the limitations of conventional complementary metal oxide semiconductor devices. Negative differential resistance (NDR) devices have been integrated with heavily doped *n*-type and *p*-type channel layers to form heterojunctions. However, undesired interfacial defects are unavoidable during heterojunction formation, and the selection of appropriate materials for type-III gap formation is constrained by the requirement for a desirable band alignment. Herein, we report the presence of NDR in WSe_2 multilayers without heterojunctions under high electrostatic drain and gate bias conditions of up to a temperature of 450 K. The peak-to-valley current ratio (PVCR) is approximately 1.2 at room temperature indicating enhanced thermal perturbation and carrier-carrier scattering. Despite an increase in the activation energy in deep metallic regimes, the observed NDR can be primarily attributed to the self-heating effect rather than band-to-band tunneling. To further exclude undesired oxide trap effects originating from SiO_2 on NDR, hexagonal boron nitride is employed as the supporting dielectric substrate with different channel lengths, achieving a PVCR of ≈2.3 with a maximum peak current of ≈58.4 μA/μm at room temperature. These findings promote the development of NDR-based multi-valued logic devices for next generation data processing and storage.

New concepts

We present multilayer tungsten diselenide transistors that exhibit negative differential resistance NDR without requiring heterointerfaces, doping, or complex heterostructures. The devices rely on self-heating, not tunnelling, to induce a lateral *p–i–n* junction under gate and drain bias, producing strong NDR with high peak current density and large peak-to-valley ratios. Unlike conventional NDR systems limited to cryogenic temperatures, our devices operate stably up to 450 K, demonstrating practical high-temperature functionality. Inverter circuits built from these transistors achieve voltage gains of up to 3.2. These findings establish self-heating as a useful mechanism in two-dimensional semiconductors, offering new strategies for thermal carrier control and enabling applications in neuromorphic computing and multi-valued logic.

1. Introduction

The recent substantial increase in data generation has necessitated optimized methodologies for managing expansive data processes and storage capacities. Although traditional complementary metal oxide semiconductor technology initially satisfied these demands by reducing the device scale and enhancing the density in line with Moore's law, further device miniaturization has introduced several challenges, including increased power consumption, interference between adjacent devices, limited storage density, and delayed signal transmission[1–6]. Consequently, various material dimensions and different types of exotic functional devices have been proposed to address these limitations[7,8]. Among them, electronic devices exhibiting a negative differential resistance (NDR) have garnered significant interest since their first development by L. Esaki in 1958[9] owing to their distinctive conduction mechanism, which offers

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advantages such as low power consumption and faster data processing[10–12].

The quantum mechanical band-to-band tunneling (BTBT) mechanism is the preferred approach for realizing NDR devices, which consist of electron-dominant *n*-type and hole-dominant *p*-type channels to form type-III broken gap heterojunctions[13]. Owing to their distinct non-monotonic carrier transport driven by quantum mechanics, NDR devices have been widely employed in numerous applications[14], including tunnel field-effect transistors (TFETs)[15], resonant tunneling diodes[16,17], radio-frequency oscillators[18], signal multipliers[19], and multi-valued logic computing[20]. In addition, with the discovery of two-dimensional (2D) materials, the integration of different materials has become more prevalent, thus tackling existing challenges in three-dimensional material-based heterointerfaces such as lattice mismatch and interfacial atomic bonding[21].

Thus far, various heterojunctions based on 2D materials have been experimentally and theoretically explored, including MoS_2/WSe_2[22,23], V-doped $WSe_2/SnSe_2$[24], ReS_2/black phosphorus (BP)[25], WS_2/SnS_2[26], and WTe_2/HfS_2[27]. Nevertheless, critical issues remain unresolved during the formation of these 2D heterojunctions, such as surface oxidation, polymer residue-induced unintentional doping, doping-related instability, and increased fabrication complexity[28]. A simple yet effective approach to address these challenges is the realization of single ambiploar 2D material-based NDR devices, as demonstrated in graphene[29], WSe_2[30,31], $MoTe_2$[32], and BP[33,34]. Meanwhile, the lack of bandgap energy in graphene[35,36], carrier-type instability in $MoTe_2$ caused by environmental conditions[37], and the high vulnerability of BP to oxygen and moisture[38,39] pose significant challenges for practical applications. Conversely, WSe_2 offers a suitable bandgap energy as a semiconductor and demonstrates a relatively high carrier mobility and stability in ambient air compared with other 2D materials. More importantly, unlike MoS_2, WSe_2 exhibits ambipolar carrier transport, allowing both electron and hole conduction depending on the electrostatic doping conditions, without severe Fermi-level pinning effects[40,41]. There advantageous properties make WSe_2 a promising candidate for high-performance NDR devices without forming heterojunctions.

In this study, we report on high-temperature NDR in *n*-type multilayer WSe_2 devices under high electrostatic gate and drain bias conditions that were sustained at temperatures up to 450 K. The strong electrostatic drain field inversed the *n*-type WSe_2 channel into a partially hole-doped region near the drain electrode, resulting in a spatially achieved *p*-*i*-*n* homojunction configuration. To gain a deeper insight into the observed NDR mechanism, we present the temperature-dependent conductance, peak-to-valley current ratio (PVCR), and peak voltage (V_{peak}) features. We found that the self-heating effect dominates the observed NDR rather than the conventional BTBT, based on the upshift of the V_{peak} with increasing temperature and the enlarged hysteresis loop as the drain bias increases. Impact ionization also occurred under high drain bias conditions. Furthermore, we fabricated WSe_2 on a hexagonal boron nitride (*h*-BN) film with different channel lengths to suppress the undesired oxide trap effects on the drain bias-dependent PVCR and hysteresis behavior, manifesting a PVCR of ≈2.3 with a maximum peak current of ≈58.4 μA/μm at room temperature. The proposed NDR device paves the way for the development of multi-valued logic devices for massive data processing and storage in memory devices[32–34] with low power consumption and a simple device architecture.

2. Results and discussions

2.1. Device structure and NDR mechanism

Figure 1a displays a false-colored scanning electron microscope (SEM) image of our multilayered WSe_2 device. The estimated channel length (*L*) and width (*W*) are 1.8 and 6.4 μm, respectively, with a maximum channel are of 11.52 μm^2. The thickness of the WSe_2 channel flakes (~9 nm) was confirmed using atomic force microscopy (AFM) (Fig. 1b). The detailed device fabrication procedures and measurement setup are described in the Methods Section. The representative optical Raman spectrum of the fabricated 9 nm-thick WSe_2 obtained with a laser wavelength of 532 nm and a power of 0.5 mW is presented in Fig. 1c. The multilayer WSe_2 flake is featured with a $\boldsymbol{E^1_{2g}}$ peak around ~249.0 cm^{-1}, $\boldsymbol{A_{1g}}$ of ~257.8 cm^{-1}, and $\boldsymbol{B^1_{2g}}$ of ~308.7 cm^{-1}, which indicate dominant vibrational modes in multilayer WSe_2 flakes, as reported in previous studies[42,43]. Additionally, the negligible changes in the dominant vibrational modes ($\boldsymbol{E^1_{2g}}$, $\boldsymbol{A_{1g}}$, and $\boldsymbol{B^1_{2g}}$) observed before and after device fabrication for WSe_2 multilayers of different thicknesses further confirm that the fabrication process did not cause significant doping or structural modifications, and that the intrinsic properties of the WSe_2 layers were well preserved, as shown in Supporting Information, Fig. S1, SEI†.

To confirm the NDR characteristics of the fabricated multilayered WSe_2 device, we measured the drain current-drain voltage (I_D-V_D) output characteristics of device #1 (WSe_2/SiO_2) at room temperature (T = 300 K) as a function of the gate voltage (V_G) (Fig. 1d). The peak voltage ($V_{peak} \approx 3$ V) and valley voltage ($V_{valley} \approx 5$ V), which represent the maximum and minimum current amplitudes in the NDR region, respectively, are clearly defined. Based on our observation, three different conduction regimes appear under different V_D conditions: (i) drift diffusion at $V_D < V_{peak}$, where electron transport is driven by both electric field (drift) and carrier concentration gradient (diffusion) under strong accumulation (Fig. 1e); (ii) NDR caused by self-heating and BTBT at $V_{peak} \leq V_D < V_{valley}$, where a temperature rise induced by Joule heating modifies carrier transport and band profile, contributing to the onset of NDR, along with BTBT, caused by hole injection from the drain (or electron depletion) that leads to the formation of a *p*–*i*–*n* homojunction (Fig. 1f); and (iii) impact ionization and/or avalanche breakdown at $V_{valley} \leq V_D$, where the increased electric field triggers strong band bending and carrier acceleration, leading to impact ionization and carrier multiplication (Fig. 1g). In particular, the non-monotonic behavior becomes prominent in the NDR regime as V_G increases, thus implying that the accumulated electrons (majority carriers) mainly contribute to the distinctive conduction, unlike conventional NDR devices caused by BTBT. Figs 1e-g illustrate the relevant conduction mechanisms of our NDR device as a function of V_D. Additionally, the output

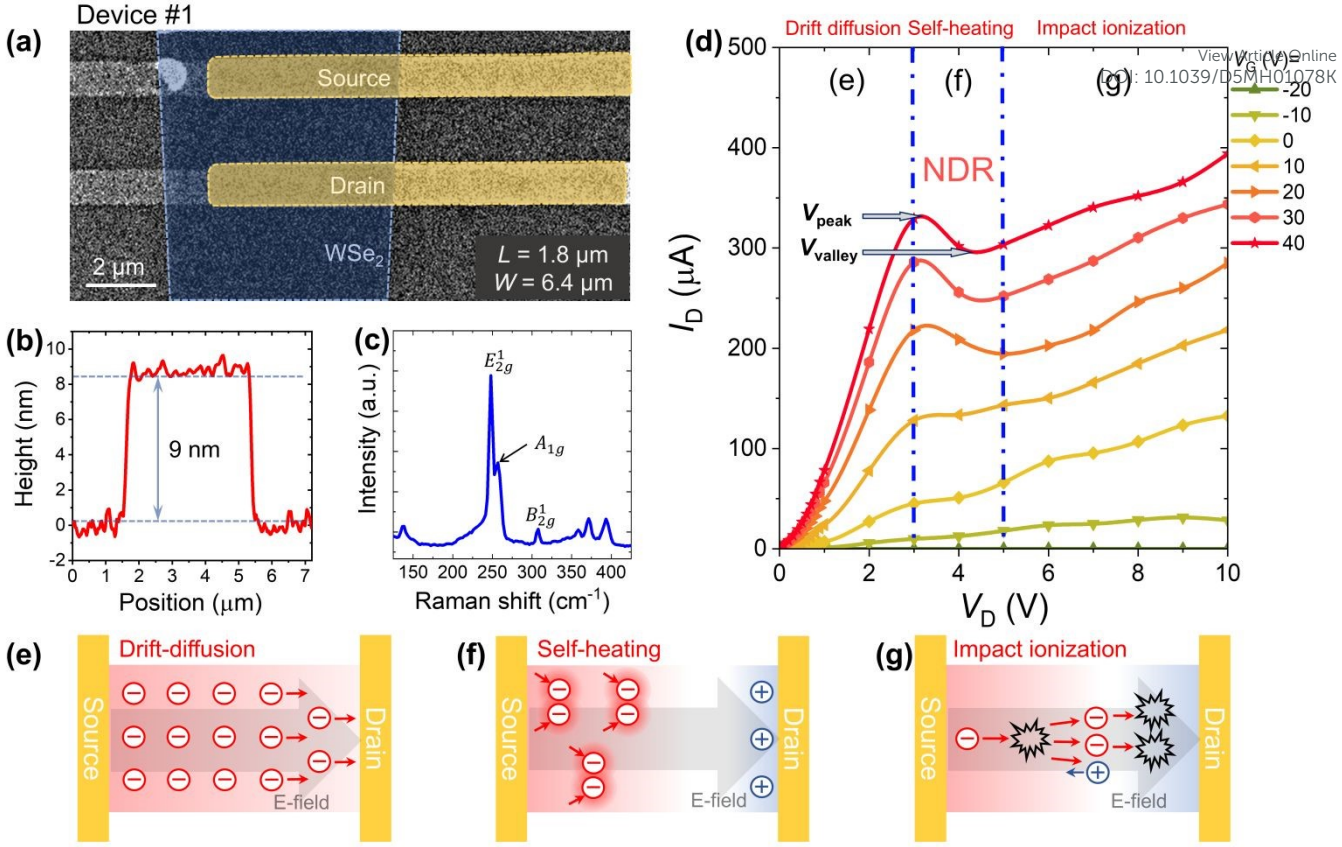

Fig. 1 Multilayered WSe_2 NDR device. (a) Optical microscopy image of the fabricated NDR device #1, where the scale bar denotes 2 μm. (b) Thickness profile of the WSe_2 multilayer channel confirmed by AFM. The thickness corresponds to 14 to 15 layers. (c) Representative optical Raman spectroscopy image of the multilayer WSe_2. (d) Output characteristic curves as a function of V_G demonstrating NDR at room temperature. The NDR phenomenon occurs under high V_D conditions above 3 V with $V_G > 20$ V. (e-g) Illustrations of different conduction mechanisms with respect to V_D: (e) drift diffusion, (f) self-heating and BTBT, and (g) impact ionization and avalanche breakdown.

characteristics of bi- and tri-layer WSe_2 were examined, including a discussion of the role of the contact buffer layer in the observed NDR behavior, as shown in Supporting Information, Fig. S2, SEI†. A detailed discussion of the origin of the observed NDR is provided in the next section.

2.2. Origin of NDR

To gain deeper insight into the carrier transport mechanism, particularly the origin of the observed NDR, the temperature-dependent output characteristic curves ranging from 300–450 K at $V_G = 20$ V are obtained, which are displayed in Fig. 2a. In general, the NDR phenomenon becomes more pronounced at lower temperatures, where a larger fraction of carrier transport occurs via quantum mechanical tunneling rather than thermionic emission, leading to an enhanced NDR signature. Additionally, reduced thermal vibrations at low temperatures increase the tunneling probability, resulting in a higher quantum yield. Nevertheless, the realization of NDR at elevated temperatures remains critical for practical applications and compatibility with existing industrial fabrication processes. Moreover, achieving high drain current density is of significant interest for high-speed, high-frequency, and high-power applications, such as microwave oscillators and power amplifiers[44,45]. The observed slope at a small V_D in Fig. 2a is close to 1, thus demonstrating a conventional transistor feature in the triode region with a nearly pseudo-ohmic contact. In addition, NDR appears consistently regardless of the temperature at V_D values ranging from 3–5 V, as shown in Fig. 1d. However, as temperature increases, NDR becomes weaker, concerning (where or corresponding) PVCR values are 1.12 (1.08) at 300 (450) K, primarily because of enhanced thermal perturbation and carrier-carrier scattering under a strong electron accumulation regime with lower turn-on voltage (V_T), ($V_T \ll V_G$), leading to significant self-heating effects as V_G increases (Fig. S3, SEI† for output characteristic curves for other V_G values). Additionally, considering the V_D-induced spatial hole-doping effects near the drain electrode in high V_D regimes[46], the contribution of BTBT to the NDR is plausible. In very high V_D regimes, impact ionization and avalanche breakdown can cause I_D to increase again, as reported in previous studies[47,48].

To explore the dominant mechanism of the observed NDR more systematically, linear-scale temperature-dependent transfer curves (I_D-V_D) at $V_D = 1$ V, corresponding to the drift diffusion regime, are obtained, which are displayed in Fig. 2b. The crossover point between the metallic (gray-shaded) and semiconducting/insulating (yellow-shaded) regions appears at $V_G \approx 20$ V (see red dashed vertical line). The corresponding 2D electron carrier density ($n_{2D} = C_{OX} \times (V_G - V_T)/q$, where C_{OX}, V_T, and q represent the oxide capacitance per unit area, turn-on voltage, and electron unit charge, respectively) is ≈6–8

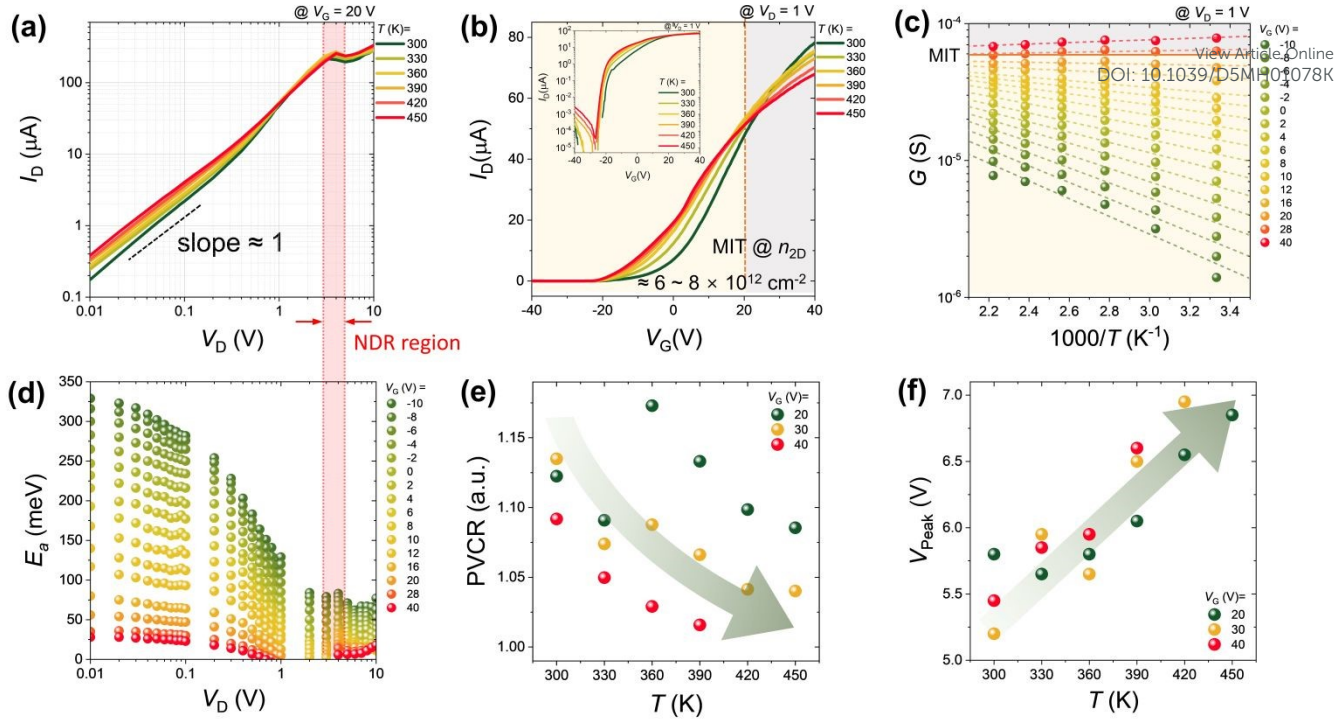

Fig. 2 Temperature-dependent NDR and PVCR. (a) *T*-dependent NDR characteristics at V_G = 20 V. NDR behavior is clearly highlighted by red-shaded areas. (b) Transfer curves as a function of *T* ranging from 300–450 K at V_D = 1 V. MIT occurs at $n_{2D} \approx 6–8 \times 10^{12}$ cm^{-2}, indicated by a red dashed line. The inset represents the corresponding semi-logarithmic scale of Figure 2b. (c) *T*- and V_G-dependence of $G(T)$ (symbols) and corresponding fitting curves (dotted lines). (d) V_D-dependent E_a as a function of V_G. The red-shaded area highlights the change in the trend of E_a where the NDR appears. Trends of (e) PCVR and (f) V_{peak} as *T* increases at V_G = 20, 30, and 40 V, respectively. Green arrows serve as guides for the eyes and avalanche breakdown.

× 10^{12} cm^{-2}. The temperature-dependent carrier concentration is displayed in Supporting Information, Fig. S4, SEI†. As reported by Moon et al., a metal–insulator transition (MIT) occurs in the 2D monolayer and multilayer MoS_2 as V_G and V_D increase[49]. Similarly, the proposed multilayer WSe_2 exhibits MIT features with varying *T*, indicating that WSe_2 is in a deep metallic regime under the V_G and V_D conditions. Fig. S5 displays the MIT features at other V_D values. Therefore, the observed NDR primarily originates from the intrinsic properties of WSe_2 rather than the Schottky barrier at the WSe_2-to-Au metal interface.

Figure 2c shows the conductance ($G(T) = I_D/V_D$) at V_D = 1 V under different V_G conditions. As V_G increases, the sign of the slope of $G(T)$ changes from negative (insulating) to positive (metallic), manifesting the MIT, as shown in Fig. 2b. The $G(T)$ data are further fitted to the thermal activation carrier transport model ($G(T) = G_0(T)\cdot\exp(-E_a/(k_B\cdot T))$, where G_0, E_a, and k_B denote the conductance prefactor for fitting, activation energy, and Boltzmann constant, respectively)[50]. The E_a reliance on V_D is plotted as a function of V_G in Fig. 2d. In general, when the channel is in the semiconducting/insulating regime (V_G < 20 V), E_a decreases as V_D increases because the Schottky barrier at the WSe_2/metal contact decreases with higher V_D. Similarly, E_a decreases with increasing V_G at a fixed V_D (for instance, V_D = 1 V) because of the increased charge carrier (electron) accumulation in the *n*-type WSe_2 channel, representing carrier drift and diffusion conduction. However, E_a increases, particularly when NDR occurs (see Figs. 3a and 3d). This increase in E_a can be ascribed to the high V_D–induced *p–i–n* configuration, which results in the formation of a BTBT barrier. By contrast, the drift velocity of the carriers significantly increases with V_D, and the populated carrier density within the WSe_2 channel leads to a higher probability of collision with the channel atoms; consequently, they generate Joule heating. Self-heating, as reported for other 2D semiconducting material[51,52] is known to contribute to NDR. Self-heating reduces the mean free path of carriers, lowering the conductivity of the channel (higher E_a), thus accounts for the observed NDR in Fig. 2a. When the carriers are further accelerated by V_D along the channel up to 10 V, the main conduction mechanism changes to the impact ionization and/or avalanche breakdown (Fig. 1g). A detailed analysis of this high V_D field region is presented in Section 2.3.

2.3. Origin of NDR hysteresis and avalanche breakdown

Here, we discuss the origin of NDR hysteresis and the potential impact ionization and/or avalanche breakdown in *n*-type WSe_2 multilayers. To this end, device #2 (WSe_2/SiO_2) was fabricated with different channel lengths (L_1/L_2 = 0.77/1.7 μm) and a width of 7.8 μm as demonstrated in Fig. 3a. The thickness of WSe_2, as confirmed by AFM, is 15 nm. Fig. 3b shows the double-swept output characteristics obtained from L_1 as a function of V_G, where hysteresis gradually appears when V_G > 0 V in the presence of NDR. Notably, negligible hysteresis is observed in the absence of NDR in small V_D regimes, regardless of V_D and V_G conditions. As presented in Fig. S6, SEI†, the negligible NDR hysteresis exhibits. In low V_D regimes, nearly zero hysteresis is observed (Fig. S6, SEI† additionally, shows multiple

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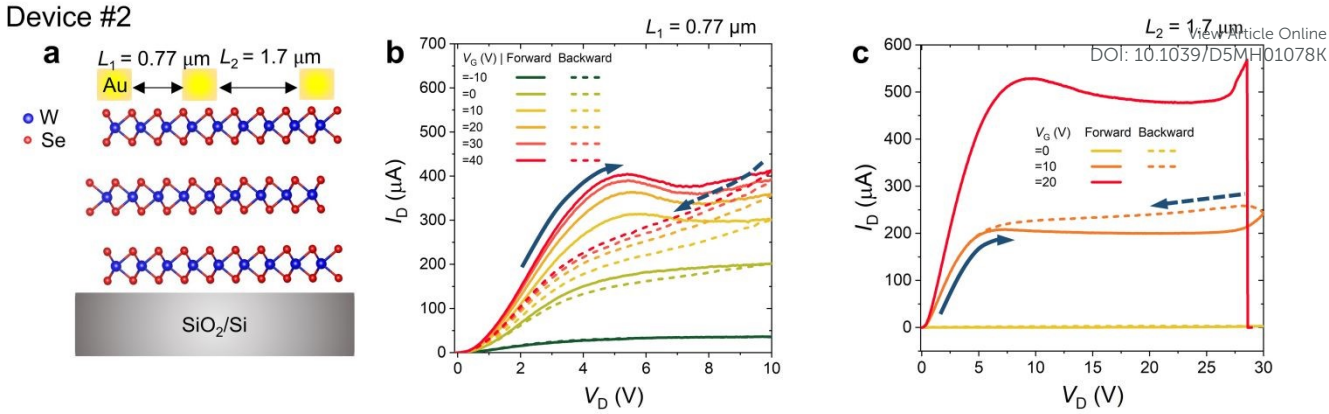

Fig. 3 Origin of NDR hysteresis and impact ionization. (a) A conceptual schematic image of device #2. The lengths of each channel are 0.77 and 1.7 μm with an identical channel width of 7.8 μm. Double sweep output characteristic curves of (b) L_1 and (c) L_2 as a function of V_G. Hysteresis behavior of NDR appears exclusively when $V_G > 0$ V (solid line: forward direction; dotted line: backward direction). The breakdown electric field is estimated to be 168 kV/cm.

double-swept output characteristic curves as a function of V_G at 1 V intervals, where the hysteresis is minimal and NDR does not occur). This is primarily because the self-heating effects are not sufficiently significant to cause NDR.

From the perspective of the various mechanisms underlying NDR, the Gunn effect could play a role beyond the conventional BTBT process and self-heating effects. In this effect, electrons are transferred from a lower valley to an upper valley with a higher effective mass (and, thus, lower carrier mobility) as V_D increases. This results in a relatively larger electron population with a higher effective mass overtaking that of the lower effective mass, reducing the channel conductivity and leading to the emergence of NDR, as previously reported by He et al[47]. However, the intervalley transition in multilayer WSe_2 is not plausible because the effective mass of the upper valley is smaller than that of the lower valley[53–55]. This is in clear contrast to the observations of this study. Furthermore, the hysteresis direction changes from counterclockwise to clockwise at V_G = 11 V, indicating possible substrate effects from fixed oxide traps when V_G is low. Consequently, the observed hysteresis appears to be closely related to the occurrence of NDR. Nevertheless, because hysteresis can generally be influenced by fixed charge traps at the WSe_2/SiO_2 interface, improving the interface conditions is essential for clarifying the relationship between the observed hysteresis and NDR. The detailed discussion will be addressed in the next section.

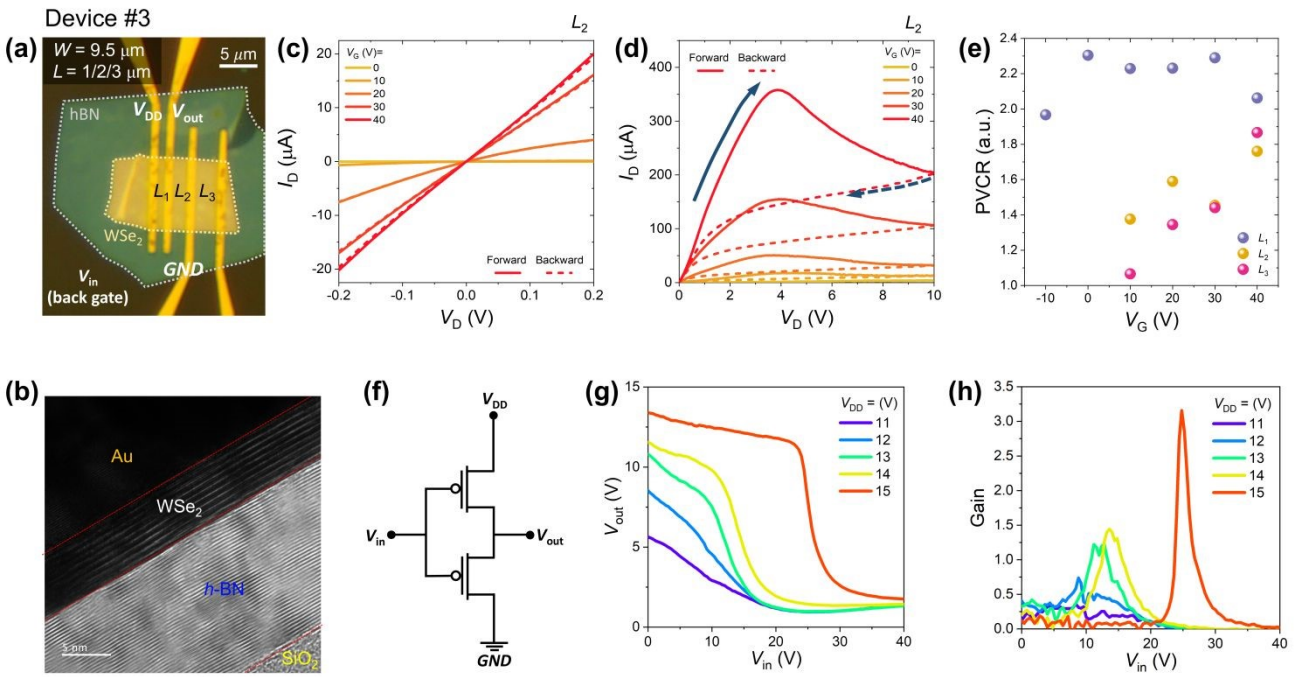

Fig. 4 NDR behavior in WSe_2/*h*-BN heterostructures and logic operation. (a) Optical (b) TEM images of the fabricated multilayer WSe_2 on the *h*-BN substrate (device #3). Scale bars represent 5 μm and 5 nm, respectively. Double-swept output characteristic curves as a function of V_G: (c) within a narrow V_D range ($|V_D| < 0.2$ V) and (d) a wide V_D range (0 V < V_D < 10 V), respectively. (e) V_G-dependent PVCR across different channel lengths. (f) The conceptual circuit diagram for our WSe_2 NDR-based inverter. (g) V_{DD}-dependent voltage transfer curves (V_{in}–V_{out}) and (h) corresponding voltage gains.

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Next, we examine the electrical characteristics near the electrical breakdown field to investigate the potential impact ionization and/or avalanche breakdown at high V_D regimes. The V_G-dependent output characteristics measured at L_2 of device #2 are presented in Fig. 3c. When V_D of up to 30 V and V_G of 10 V are applied, the forward current exhibits an NDR at $V_D \approx 28.5$ V. The corresponding field across the L_2 channel is estimated to be approximately 168 kV/cm, which is comparable to the values reported for other 2D materials such as MoS_2, WS_2, and WSe_2[46–48]. Carrier multiplication occurs with a high carrier velocity when a strong lateral field accelerates a sufficient number of carriers to generate additional carriers from lattice atoms through impact ionization. The observed I_D shows an abrupt increase at $V_D \approx 25$ V and rapidly drops to zero at approximately 28.5 V when $V_G = 20$ V. This feature is attributed to the intense heat generation from the extremely high field at which the thermal stability of the fabricated semiconducting WSe_2 is exceeded, resulting in channel breakdown or burnout[46].

2.4. NDR in WSe_2/*h*-BN heterostructures

To achieve a clean interface at WSe_2/SiO_2 and, more importantly, to exclude the undesired oxide trap effect on the observed NDR hysteresis, we employed multilayer *h*-BN dielectrics owing to their chemically inert properties, atomically smooth surface, and high stability[56,57]. A representative optical image of the fabricated device #3 (WSe_2/*h*-BN/SiO_2) is displayed in Fig. 4a, where the channel lengths and width are defined as $L_1/L_1/L_1 = 1/2/3$ μm and $W = 9.5$ μm, respectively. The thicknesses of *h*-BN and WSe_2, as measured by transmission electron microscopy (TEM), are approximately 14.6 nm and 6 nm, respectively. The WSe_2 thickness corresponds to ~9 layers, assuming an interlayer spacing of ~0.65 nm. A sharp interface between *h*-BN and WSe_2 is clearly observed, suggesting negligible top-surface oxidation of WSe_2 during device fabrication. Figs S7-8, SEI† provide detailed device and material information obtained from non-contact AFM analyses, along with focused ion beam and additional TEM images, conforming the absence of heterojunction formation in Device #3 shown in Fig. 4a. Electrical measurements are performed under low vacuum ($\approx 10^{-3}$ torr) conditions without thermal annealing process. Fig. 4c represents the double-swept output characteristics of device #3 as a function of V_G, measured at L_2. At $|V_D| < 0.2$ V, the obtained I_D is nearly proportional to V_D with zero-hysteresis, manifesting a pseudo-ohmic behavior owing to a reduced contact resistance and Schottky barrier height achieved by inserting *h*-BN multilayers at the interface between WSe_2 and SiO_2[58].

The V_G-dependent NDR and hysteresis features of device #3 over a wide V_D range of 0–10 V are presented in Fig. 4d. In contrast to the hysteresis observed in Fig. 4c, NDR gradually appears with increasing V_G, and the hysteresis becomes more pronounced with decreasing V_D. Considering the reported strong self-heating effects of *h*-BN on 2D multilayers, it is evident that the larger hysteresis can be primarily ascribed to the use of *h*-BN, which further reduces the valley current (or effective conductivity). Consequently, this increase in the PVCR to approximately 2.3, along with a high peak current density of ≈58.4 μA/μm, is achieved by effectively preventing undesired carrier scattering contributions to the observed NDR stemming from SiO_2. Fig. 4e shows the corresponding PVCR as a function of the channel length. The PVCR reaches its highest value with L_1, regardless of V_G values. At $V_G = -10$ and 0 V, the PVCR is not defined as the I_{peak} at L_2, and L_3 is not found under these bias conditions. These findings provide deeper insights into the working mechanisms of quantum electrical devices.

Furthermore, we evaluated the logic functionality of our NDR device through inverter measurements. The conceptual circuit diagram is illustrated in Fig. 4f, where V_{DD}, V_{out}, V_{in}, and GND denote supply voltage, output voltage, input voltage, and ground, respectively, as indicated in Fig. 4a. V_{in} was applied via the back-gate, consisting of a bottom *h*-BN and SiO_2 dielectric stack. Fig. 4g demonstrates the voltage transfer characteristics with V_{in} from 0 to 40 V under various V_{DD} values ranging from 11 to 15. A clear switching response becomes more evident with increasing V_{DD}, manifesting logic operation. The corresponding voltage gain, presented in Fig. 4h,

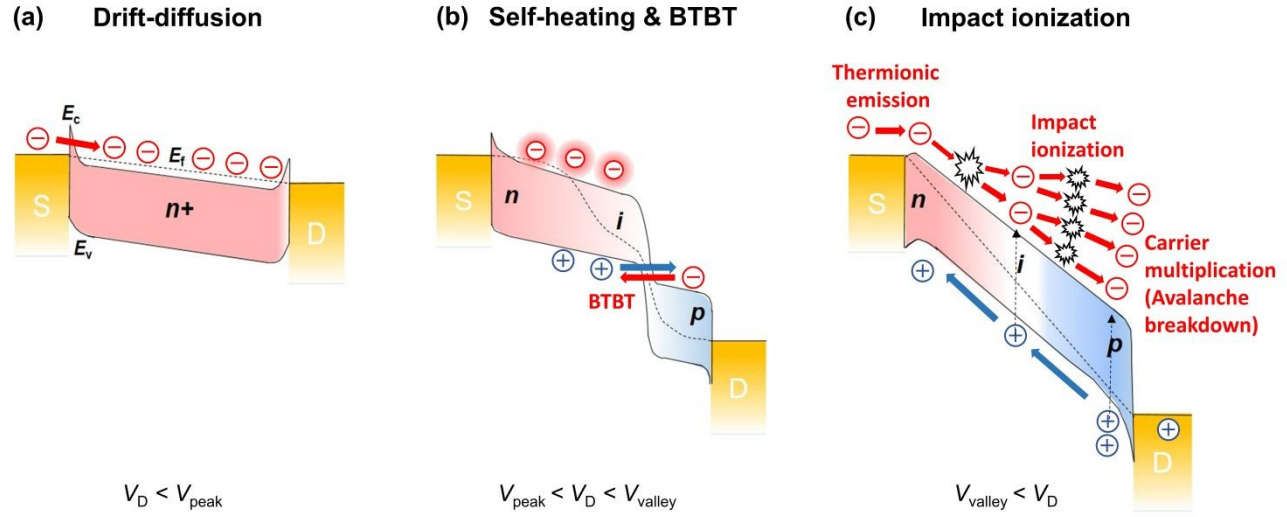

Fig. 5 Conceptual energy diagrams for the fabricated multilayer *n*-type WSe_2 illustrating different conduction mechanisms under strong electron accumulation across varying V_D conditions. (a) At low $V_D < V_{peak}$, drift diffusion dominates. (b) At $V_{peak} < V_D < V_{valley}$, NDR occurs by self-heating and BTBT, forming an *n–i–p* homojunction. (c) At $V_{valley} < V_D$, impact ionization and/or avalanche carrier multiplication.

exceeds 3.15 at V_{DD} = 15V. These results highlight the potential of 2D homojunction-based NDR devices for future logic applications.

Finally, to provide a clearer picture of the NDR mechanism in our multilayered WSe_2 devices, conceptual energy diagrams are illustrated in Fig. 5 for various V_D ranges (also see Figs. 1e–g). At high electron accumulation regime ($V_G > V_T$), the diffusion and drift carrier transport mechanisms dominate our *n*-type WSe_2 under a low V_D ($0 < V_D < V_{peak}$), with a uniform distribution of carrier density (see Fig. 5a). As V_D increases ($V_{peak} < V_D < V_{valley}$), more hole carriers are injected from the drain electrode (or electrons are depleted near the drain electrode), resulting in a *p–i–n* homojunction structure that initiates a partial BTBT process along with self-heating effects[33,34,46,59–62]. With a further increase in V_D ($V_{valley} < V_D$), the energy band bends more severely, reducing the height and thickness of the barriers at the source and drain electrodes. The electrons injected from the source are then accelerated by the high lateral field (steep-energy bending) and collide with other electrons, generating additional carriers. These newly generated carriers accelerate and collide with the nearby electrons. This consecutive event leads to carrier multiplication, which increases the overall carrier population within WSe_2[43]. Breakdown occurs upon a further increase in V_D. To benchmark the observed NDR features in this study, we compared the width-normalized peak drain current (I_D/W) and PVCR with the values from previous studies on 2D heterojunction- and homojunction-based NDR devices (see Fig. 6)[22,23,24–26,30–33,47,63–65]. We note that the highest values of I_{peak} and PVCR from each reference were taken for fair performance comparison. Devices with a small I_{peak} density and PVCR have their NDR behavior masked by undesired electrical noise and parasitic effects. Meanwhile, NDR devices with high I_{peak} density and large PVCR ensure the distinctive and improved noise immunity, improving the reliability and robustness in practical applications including voltage-controlled oscillators demanding high current density for high voltage output[66].

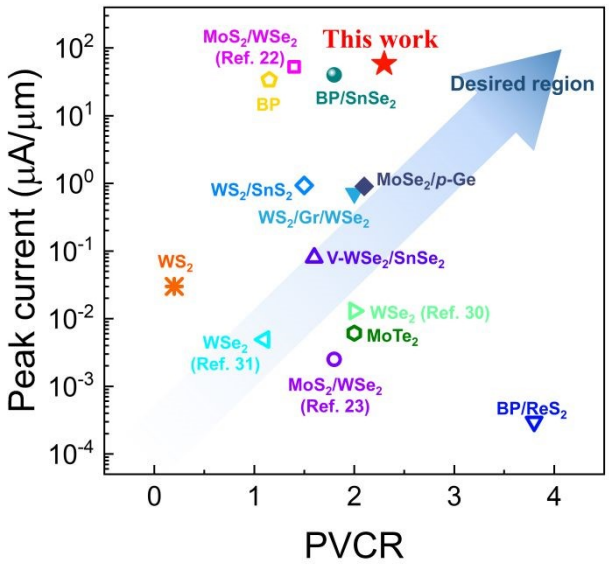

Fig. 6 Benchmark of the width-normalized peak current and PVCR obtained from previously reported 2D heterojunction- and homojunction-based NDR devices. Our multilayer WSe_2 homojunction NDR device exhibits a high peak current density and PVCR exceeding 58.4 μA/μm and 2.3, respectively.

3. Conclusions

In summary, we successfully demonstrated high-temperature NDR devices using *n*-type WSe_2 multilayers without heterojunctions operating from room temperature to 450 K under high electrostatic drain and gate bias conditions. These devices exhibit high thermal stabilities, making them suitable for pragmatic applications in high-temperature environments. We achieved a PVCR of ≈2.3 with a maximum peak current of ≈58.4 μA/μm in the WSe_2/h-BN device, comparable to those of other BTBT-based TFETs. When h-BN is used as the substrate, the NDR hysteresis becomes more pronounced, thus confirming that self-heating is the primary origin of the observed hysteresis, whereas surface trap-induced hysteresis is largely suppressed. We found that the key mechanism of our NDR device is self-heating, distinguishing it from conventional TFETs that rely on BTBT and intervalley transitions. The electrically tunable spatial doping profile of the channel forms a homojunction within the material, thereby controlling the conduction mechanism without the need for complicated extrinsic doping or integration processes. Finally, a large current under high bias conditions contributes to the impact ionization and/or avalanche breakdown for further high-voltage applications. Our findings demonstrate the potential of high-performance junctionless multivalued logic devices for next-generation data processing and storage applications.

4. Methods

4.1. Fabrication of multilayered WSe_2 homojunction NDR devices

Commercialized bulk WSe_2 flakes (HQ Graphene) were first mechanically cleaved onto polydimethylsiloxane (Gel Pak) sheets using an adhesive Scotch tape. The exfoliated WSe_2 flakes were identified *via* optical contrast using optical microscopy. WSe_2 flakes with the proper thickness were then aligned and transferred onto a 90 nm SiO_2/p^+-Si substrate using a dry transfer machine (DTS-P200, WIT). The top electrodes were designed and patterned using conventional electron-beam lithography (MIRA3, TESCAN, and Elphy Quantum, Raith) with a bilayer of poly(methylmethacrylate) (EL11 and C4; Kayaku Advanced Materials). A 100-nm-thick metal (Au) layer was deposited for contact *via* electron beam evaporation (INFOVION) at a deposition rate of 0.5 Å/s, followed by a lift-off process in a warm acetone bath for 30 min.

4.2. Raman spectroscopy

The optical Raman spectra were investigated using a confocal Raman spectroscope (XperRam Compact, NANOBASE) with a laser excitation wavelength of 532 nm and a power of 0.5 mW. The laser beam was focused onto the sample by using a 40× objective lens with a numerical aperture of 0.75. The focused light was analyzed via spectrometer (XPE 35) with a grating option of 600 lpmm.

4.3. Transmission electron microscopy and scanning probe microscopy

The thickness profile was confirmed using TEM (JEM-ARM200F, JEOL) operated at 200 kV in Cs-corrected scanning TEM mode. The sample was prepared by focused ion beam milling using a dual-beam system (Helios G4 UC, Thermo Fisher Scientific). The topography of the complete device was characterized using AFM (NX10, Park Systems Inc.) in a tapping mode. XEI software was used for extracting the flake's height information by the thickness difference between substrate and target flakes.

4.4. Electrical characterization

All electrical characterizations were performed using a semiconductor analyzer (B1500A, Keysight). The *I–V* characteristics were measured under various V_D conditions in a vacuum environment with a chamber pressure of $\approx 5.0 \times 10^{-6}$ torr. Temperature-dependent *I–V* measurements were performed using a temperature controller, with temperatures ranging from 300–450 K.

Author contributions

H.K., T.K., and Y.H. contributed equally to this work. H.K., T.K., Y.H., M.C., and M.-K.J. conceived and designed the experiments with the help of J.S.K., A.C., and C.T. H.K., Y.H., and M.C. fabricated the devices with the help of D.C., E.S., S.S., M.C., and E.C. H.K., T.K., Y.H., and M.C. carried out the transport measurements including temperature-dependent electrical properties and inverter characteristics. H.K. and S.S. conducted FIB, TEM, and AFM analysis. H.K., T.K., Y.H., C.K., A.C., C.T., and M.-K.J. performed the data analysis. H.K., T.K., Y.H., A.C., C.T., and M.-K.J. wrote the manuscript. M.-K.J. supervised the project. All authors discussed the results and reviewed the manuscript.

Conflicts of interest

The authors declare no conflict of interest.

Data availability

The data supporting this article have been included as part of the Supplementary Information.

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References

1 G. E. Moore, *Proc. IEEE*, 1998, **86**, 82–84.
2 Y. Liu, X. Duan, H. J. Shin, S. Park, Y. Huang and X. Duan, *Nature*, 2021, **591**, 43–53.
3 D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur and H. S. P. Wong, *Proc. IEEE*, 2001, **89**, 259–287.
4 T. Wei, Z. Han, X. Zhong, Q. Xiao, T. Liu and D. Xiang, *iScience*, 2022, **25**, 105160.
5 Y. Shen, Z. Dong, Y. Sun, H. Guo, F. Wu, X. Li, J. Tang, J. Liu, X. Wu, H. Tian and T. L. Ren, *Adv. Mater.*, 2022, **34**, 2201916.
6 M. K. Joo, *Appl. Sci. Converg. Technol.*, 2023, **32**, 41–44.
7 X. Huang, C. Liu, Z. Tang, S. Zeng, L. Liu, X. Hou, H. Chen, J. Li, Y. G. Jiang, D. W. Zhang and P. Zhou, *Tech. Dig. - Int. Electron Devices Meet. IEDM*, 2020, **2020**-**Decem**, 12.1.1-12.1.4.
8 S.-Y. Lee, S. M. Kim, E.-J. Yoon, C.-W. Oh, I. Chung, D. Park and K. Kim, *IEEE Trans. Nanotechnol.*, 2003, **2**, 253–257.
9 L. Esaki, *Phys. Rev.*, 1958, **109**, 603–604.
10 H. K. Sung, H. Kam, C. Hu and T. J. K. Liu, *Dig. Tech. Pap. - 2009 Symp. VLSI Technol.*, 2009, 178–179.
11 I. C. Cherik, S. Mohammadi and S. K. Maity, *Sci. Rep.*, 2023, **13**, 1–12.
12 H. Lu and A. Seabaugh, *IEEE J. Electron Devices Soc.*, 2014, **2**, 44–49.
13 V. O. Özçelik, J. G. Azadani, C. Yang, S. J. Koester and T. Low, *Phys. Rev. B*, 2016, **94**, 035125.
14 S. Kanungo, G. Ahmad, P. Sahatiya, A. Mukhopadhyay and S. Chattopadhyay, *npj 2D Mater. Appl.*, DOI:10.1038/s41699-022-00352-2.
15 S. Aftab, H. M. S. Ajmal, E. Elahi, H. M. Mansoor Ul Haque, Samiya, M. W. Iqbal, J. Aziz, S. Yousuf, M. Z. Iqbal and M. A. Shehzad, *ACS Appl. Nano Mater.*, 2022, **5**, 6455–6462.
16 Y. C. Lin, R. K. Ghosh, R. Addou, N. Lu, S. M. Eichfeld, H. Zhu, M. Y. Li, X. Peng, M. J. Kim, L. J. Li, R. M. Wallace, S. Datta and J. A. Robinson, *Nat. Commun.*, 2015, **6**, 4–9.
17 K. Kim, N. Prasad, H. C. P. Movva, G. W. Burg, Y. Wang, S. Larentis, T. Taniguchi, K. Watanabe, L. F. Register and E. Tutuc, *Nano Lett.*, 2018, **18**, 5967–5973.
18 A. M. Askar, P. Palacios, F. Pasadas, M. Saeed, M. R. Mohammadzadeh, R. Negra and M. M. Adachi, *npj 2D Mater. Appl.*, 2023, **7**, 1–11.
19 A. Nourbakhsh, A. Zubair, M. S. Dresselhaus and T. Palacios, *Nano Lett.*, 2016, **16**, 1359–1366.
20 S. S. Teja Nibhanupudi, A. Roy, D. Veksler, M. Coupin, K. C. Matthews, M. Disiena, Ansh, J. V. Singh, I. R. Gearba-Dolocan, J. Warner, J. P. Kulkarni, G. Bersuker and S. K. Banerjee, *Nat. Commun.*, DOI:10.1038/s41467-024-46372-y.
21 K. S. Kim, J. Kwon, H. Ryu, C. Kim, H. Kim, E.-K. Lee, D. Lee, S. Seo, N. M. Han, J. M. Suh, J. Kim, M.-K. Song, S. Lee, M. Seol and J. Kim, *Nat. Nanotechnol.*, 2024, **19**, 895–906.
22 J. H. Kim, S. Sarkar, Y. Wang, T. Taniguchi, K. Watanabe and M. Chhowalla, *Nano Lett.*, 2024, **24**, 2561–2566.

23 T. Roy, M. Tosun, X. Cao, H. Fang, D. H. Lien, P. Zhao, Y. Z. Chen, Y. L. Chueh, J. Guo and A. Javey, *ACS Nano*, 2015, **9**, 2071–2079.
24 S. Fan, S. J. Yun, W. J. Yu and Y. H. Lee, *Adv. Sci.*, 2020, **7**, 1–8.
25 J. Shim, S. Oh, D. H. Kang, S. H. Jo, M. H. Ali, W. Y. Choi, K. Heo, J. Jeon, S. Lee, M. Kim, Y. J. Song and J. H. Park, *Nat. Commun.*, 2016, **7**, 1–8.
26 J. Wang, R. Jia, Q. Huang, C. Pan, J. Zhu, H. Wang, C. Chen, Y. Zhang, Y. Yang, H. Song, F. Miao and R. Huang, *Sci. Rep.*, 2018, **8**, 1–9.
27 C. Lei, Y. Ma, X. Xu, T. Zhang, B. Huang and Y. Dai, *J. Phys. Chem. C*, 2019, **123**, 23089–23095.
28 R. Neshati, in *2013 Proceedings of PICMET 2013: Technology Management in the IT-Driven Services*, PICMET, 2013, pp. 2757–2764.
29 Y. Wu, D. B. Farmer, W. Zhu, S. J. Han, C. D. Dimitrakopoulos, A. A. Bol, P. Avouris and Y. M. Lin, *ACS Nano*, 2012, **6**, 2610–2616.
30 T. Lee, K. S. Jung, S. Seo, J. Lee, J. Park, S. Kang, J. Park, J. Kang, H. Ahn, S. Kim, H. W. Lee, D. Lee, K. S. Kim, H. Kim, K. Heo, S. Kim, S. H. Bae, S. Kang, K. Kang, J. Kim and J. H. Park, *Adv. Mater.*, 2024, **36**, 1–11.
31 S. Seo, J. Koo, J.-W. Choi, K. Heo, M. Andreev, J.-J. Lee, J.-H. Lee, J.-I. Cho, H. Kim, G. Yoo, D. H. Kang, J. Shim and J.-H. Park, *npj 2D Mater. Appl.*, DOI:10.1038/s41699-021-00213-4.
32 Y. Tang, L. Gan, J. Feng, Y. Li, Y. Zhong and C. Z. Ning, in *2023 Opto-Electronics and Communications Conference, OECC 2023*, IEEE, 2023, pp. 1–2.
33 R. Cheng, L. Yin, R. Hu, H. Liu, Y. Wen, C. Liu and J. He, *Adv. Mater.*, 2021, **33**, 1–8.
34 Y. Kim, C. Kim, S. Y. Kim, B. C. Lee, Y. Seo, H. Cho, G.-T. Kim and M.-K. Joo, *Adv. Funct. Mater.*, 2022, **32**, 2110391.
35 C. Berger, Z. Song, X. Li, X. Wu, N. Brown, C. Naud, D. Mayou, T. Li, J. Hass, A. N. Marchenkov, E. H. Conrad, P. N. First and W. A. De Heer, *Science (80-.).*, 2006, **312**, 1191–1196.
36 M. I. Katsnelson, K. S. Novoselov and A. K. Geim, *Nat. Phys.*, 2006, **2**, 620–625.
37 B. Chen, H. Sahin, A. Suslu, L. Ding, M. I. Bertoni, F. M. Peeters and S. Tongay, *ACS Nano*, 2020, **9**, 5326–5332.
38 M.-H. Jeong, D.-H. Kwak, H.-S. Ra, A.-Y. Lee and J.-S. Lee, *ACS Appl. Mater. Interfaces*, 2018, **10**, 19069–19075.
39 A. Favron, E. Gaufrès, F. Fossard, A. L. Phaneuf-Laheureux, N. Y. W. Tang, P. L. Lévesque, A. Loiseau, R. Leonelli, S. Francoeur and R. Martel, *Nat. Mater.*, 2015, **14**, 826–832.
40 K. Sotthewes, R. Van Bremen, E. Dollekamp, T. Boulogne, K. Nowakowski, D. Kas, H. J. W. Zandvliet and P. Bampoulis, *J. Phys. Chem. C*, 2019, **123**, 5411–5420.
41 J. Jang, H.-S. Ra, J. Ahn, T. W. Kim, S. H. Song, S. Park, T. Taniguch, K. Watanabe, K. Lee and D. K. Hwang, *Adv. Mater.*, 2022, **34**, 1–8.
42 R. Zhang, D. Drysdale, V. Koutsos and R. Cheung, *Adv. Funct. Mater.*, 2017, **27**, 1702455.
43 Y. Han, M. Chae, D. Choi, I. Song, C. Ko, A. Cresti, C. Theodorou and M.-K. Joo, *ACS Appl. Mater. Interfaces*, 2023, **15**, 58605–58612.
44 S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices: Third Edition*, 2006.
45 A. M. Ionescu and H. Riel, *Nature*, 2011, **479**, 329–337.
46 J. Kim, K. Cho, J. Pak, W. Lee, J. Seo, J. K. Kim, J. Shin, J. Jang, K. Y. Baek, J. Lee, S. Chung, K. Kang and T. Lee, *ACS Nano*, 2022, **16**, 5376–5383.
47 G. He, J. Nathawat, C. P. Kwan, H. Ramamoorthy, R. Somphonsane, M. Zhao, K. Ghosh, U. Singisetti, N. Perea-López, C. Zhou, A. L. Elías, M. Terrones, Y. Gong, X. Zhang, R. Vajtai, P. M. Ajayan, D. K. Ferry and J. P. Bird, *Sci. Rep.*, 2017, **7**, 1–9.
48 J. Pak, Y. Jang, J. Byun, K. Cho, T.-Y. Kim, J.-K. Kim, B. Y. Choi, J. Shin, Y. Hong, S. Chung and T. Lee, *ACS Nano*, 2018, **12**, 7109–7116.
49 B. H. Moon, J. J. Bae, M.-K. Joo, H. Choi, G. H. Han, H. Lim and Y. H. Lee, *Nat. Commun.*, 2018, **9**, 1–8.
50 M. Chae, S. Kim, Y. Han, D. Choi, Y. Choi, H. Kim and M.-K. Joo, *Appl. Sci. Converg. Technol.*, 2022, **31**, 85–88.
51 W. Dang, Y. Huangfu, M. Hossain, X. Lin, Z. Lu, Z. Huang, Z. Li, Y. Liu and X. Duan, *ACS Appl. Electron. Mater.*, 2024, **6**, 472–477.
52 X. Shi, X. Li, Q. Guo, H. Gao, M. Zeng, Y. Han, S. Yan and Y. Wu, *Nano Lett.*, 2022, **22**, 7667–7673.
53 A. Kormányos, G. Burkard, M. Gmitra, J. Fabian, V. Zólyomi, N. D. Drummond and V. Fal'ko, *2D Mater.*, 2015, **2**, 022001.
54 R. Perea-Causin, S. Brem, O. Schmidt and E. Malic, *Phys. Rev. Lett.*, 2024, **132**, 36903.
55 C. E. Mørch Nielsen, F. Fischer and G. Bester, *npj 2D Mater. Appl.*, 2025, **9**, 1–6.
56 M.-K. Joo, B. H. Moon, H. Ji, G. H. Han, H. Kim, G. Lee, S. C. Lim, D. Suh and Y. H. Lee, *Nano Lett.*, 2016, **16**, 6383–6389.
57 C. R. Dean, A. F. Young, I. Meric, C. Lee, L. Wang, S. Sorgenfrei, K. Watanabe, T. Taniguchi, P. Kim, K. L. Shepard and J. Hone, *Nat. Nanotechnol.*, 2010, **5**, 722–726.
58 D. Choi, M. Chae, Y. Han and M.-K. Joo, *Appl. Phys. Lett.*, 2024, **124**, 093504.
59 S. Berweger, G. Qiu, Y. Wang, B. Pollard, K. L. Genter, R. Tyrrell-Ead, T. M. Wallis, W. Wu, P. D. Ye and P. Kabos, *Nano Lett.*, 2019, **19**, 1289–1294.
60 M. H. Bae, Z. Y. Ong, D. Estrada and E. Pop, *Nano Lett.*, 2010, **10**, 4787–4793.
61 G. Long, Y. Wang, T. Bai, W. Li, P. Zhang, X. Deng, X. Cai, M. Xi, Y. Lin, X. Cheng, C. Fan, F. Xia, X. Luo, Z. Zhang, X. Liang, Z. Zhang, N. Sun, L. M. Peng and Y. Hu, *Nat. Commun.* , 2025, **16**, 1–11.
62 M. Freitag, H. Y. Chiu, M. Steiner, V. Perebeinos and P. Avouris, *Nat. Nanotechnol.*, 2010, **5**, 497–501.
63 R. Yan, S. Fathipour, Y. Han, B. Song, S. Xiao, M. Li, N. Ma, V. Protasenko, D. A. Muller, D. Jena and H. G. Xing, *Nano Lett.*, 2015, **15**, 5791–5798.
64 W. Uddin, V. Dhyani, G. Ahmad, V. Kumar, P. K. Muduli and S. Das, *ACS Appl. Electron. Mater.*, 2020, **2**, 1567–1573.

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65 J. H. Lim, J. Shim, B. S. Kang, G. Shin, H. Kim, M. Andreev, K. S. Jung, K. H. Kim, J. W. Choi, Y. Lee and J. H. Park, *Adv. Funct. Mater.*, 2019, **29**, 1–8.
66 S. Huo, H. Qu, F. Meng, Z. Zhang, Z. Yang, S. Zhang, X. Hu and E. Wu, *Nano Lett.*, 2024, **24**, 11937–11943.